HT32 MCU Hardware Development Guideline

D/N: AN0630EN

Introduction

This application note provides HT32 MCU system designers with relevant information regarding hardware implementation, including circuit board functions such as power, clock management, reset, boot mode settings, debug management and so on. It introduces how to use the HT32 MCUs and describes the minimum hardware resources required for actual applications. The purpose is to assist users who are new to the HT32 MCUs to quickly implement their corresponding circuit design.

Power and Reset of HT32 Series

The MCU power scheme varies according to different devices, therefore the actual conditions and parameters should be obtained from the corresponding datasheet and user manual.

Power

- V_{DD}

  V_{DD} is the power source for the internal voltage regulator, I/O pins, reset circuits, power management and clock circuits (see Note 2 and 3). It is supplied through the external VDD/VDDA pin which needs to be connected to a bypass capacitor. The V_{DD} power operating voltage range can be obtained from the datasheet. The voltage generated by the internal voltage regulator (e.g. 1.5V or 1.8V, Note 1) supplies power to the core power domain V_{CORE}. For the MCU types with an internal USB regulator, the internal USB regulator output can supply power to USB PHY.

  Note 1: Refer to the corresponding datasheet and user manual for the actual parameter values.

  Note 2: For newly released MCU types, the high speed internal oscillator is supplied by the core power domain V_{CORE}.

  Note 3: For MCU types which have a VBAT pin, refer to the V_{BAK} description.

- V_{DDIO}

  For MCU types which have a VDDIO pin, there are a group of I/O pins that can be independently powered. The pin assignment diagram in the datasheet can be used to obtain details about the structure of each I/O pin. The V_{DDIO} voltage can be different from V_{DD}, therefore the I/O pins in the V_{DDIO} domain can be directly connected to external devices that are not powered by the V_{DD} level to remove the need for level shifting circuits. The VDDIO pin needs to be connected to a bypass capacitor. The operating voltage range can be obtained from the datasheet.

- V_{BAK}

  There is a backup power domain V_{BAK} in the MCU types which have a VBAT pin. The backup power domain, V_{BAK}, provides power to the low speed internal oscillator, LSI, low speed external crystal oscillator, LSE, power management, backup registers, etc. This means that when the V_{DD} is turned off the contents of the backup registers will be retained and the RTC circuit, power management circuit and low speed clock circuits can continue running. The operating voltage range of the backup domain can be obtained from the datasheet.

  Note: The VBAT pin must not be allowed to float. When the backup power is not used, the VBAT pin must be connected to the VDD pin. A special case, is for the HT32F52352 which is supplied in the 33 QFN package, where the VBAT pin is not externally bounded. Here, for pins 13, 14 and 15 which are the backup power domain pins, a 100Ω resistor should be connected between the pins and VDD. This will ensure that VBAT has power, which is implemented by the internal ESD protection diode connected to V_{BAK}.

- LDO

  An internal voltage regulator generates a 1.5V or 1.8V voltage which is provided to the core power domain, V_{CORE}. The output pin, CLDO, should be connected with an external capacitor whose value can be obtained from the CLDO pin description in the corresponding datasheet. The LDO has several power modes, which can be obtained from the PWRCU section of the corresponding datasheet.

- USB LDO

  An internal USB regulator output can provide power to USB PHY. The VREGO output pin should be connected with an external capacitor whose value can be obtained from the VREGO pin description in the corresponding datasheet. Because the MCU power schemes vary with different types of the MCU, refer to the corresponding datasheet and user manual for the actual parameters. The output voltage of the USB regulator can be configured based on actual requirements. Refer to the PWRCR register description in the PWRCU section for the configuration and voltage ranges.

- V_{LCD}

  For the MCU types with an integrated segment code LCD peripheral, V_{LCD} provides power to most of the LCD circuits, including the COM & SEG drivers, analog switches/MUX, resistor ladder network and so on. The V_{LCD} voltage can be supplied by either an external power source or the internal charge pump circuit. When the internal charge pump is selected to provide the LCD power, the VLCD pin must be connected to a 2.2μF capacitor which should be located as close as possible to the VLCD and VSS pins. If V_{LCD} is supplied by external power, the VLCD pin must be connected to a bypass capacitor.

- V_{DDA}

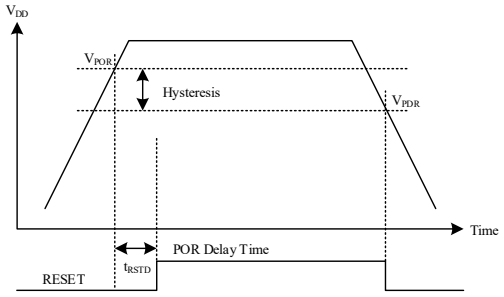
  V_{DDA} is the analog power for the A/D converters, D/A converters, voltage reference buffers, and comparators. V_{DDA}, which is supplied by the VDDA pin, must be equal to the V_{DD} value, see the note below. If any analog circuit mentioned above is used, it is recommended to add a 2.2μF regulation capacitor in parallel with a 0.1μF bypass capacitor or connect a normal bypass capacitor. The V_{DDA} operating voltage range can be obtained from the ADC, DAC, CMP and VREF electrical characteristics in the datasheet.

Note: Some MCU types allow the condition whereby $V_{DDA} \leq V_{DD}$. For details about this, refer to the corresponding datasheet.

Reset

- Power-on reset

The power-on reset, (POR) is generated by an internal reset generator which has an internal filter to avoid erroneous operation caused by noise. The HT32 MCUs have integrated POR and PDR circuits. The reset signal is valid when the system is powered on. When V_{DD} exceeds V_{POR} and after a t_{RSTD} time, the reset will be disabled and the MCU will begin to operate normally. During normal operation, if V_{DD} drops below the V_{PDR} value, the reset circuit will reset the MCU immediately to prevent the device from malfunctioning at a low voltage. The V_{POR} and V_{PDR} voltage values can be obtained from the V_{DD} power reset characteristics of the datasheet.



- System reset

The system reset is generated by the power-on reset PORRESETn, watchdog timer reset WDT_RSTn, nRST pin, or a software reset SYSRESETREQ event.

◆ WDT reset

The watchdog timer is a hardware timing circuit that is used to detect a system freeze caused by a software deadlock. The watchdog timer can work in the reset mode. When the watchdog counter counts down to the zero, the watchdog timer will generate a reset. Therefore, during normal operation the software should reload the counter value before the watchdog timer underflows. In addition, if the software reloads the counter before the counter reaches the WDT delta value, a reset can also occur. This aims to prevent the software from being stuck in software areas where the counter is being constantly reloaded. Therefore the counter must be reloaded during the limited time window where the watchdog timer value is from 0 to WDTD.

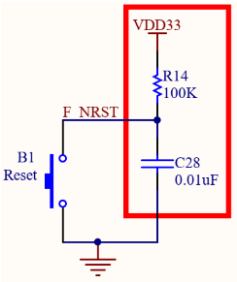
The watchdog timer counter can be stopped when the processor is in the debug or sleep mode. In order to prevent the watchdog timer configuration from being changed unexpectedly, the write protection for the register should be enabled.

◆ Software reset - NVIC Reset

A reset request is sent to the system through the NVIC. Refer to the Cortex®-M0+ technical reference manual for more information.

◆ nRST pin reset

When the nRST pin inputs a low level, the MCU will reset most of the registers. This reset ends when the nRST pin changes from a low level to a high level. It should be noted that the RTC, PWRCU registers and backup registers will not be reset. As shown below, it is recommended that the nRST pin is connected to a 100kΩ pull-up resistor and a 0.01μF capacitor. The specific values can be adjusted according to actual requirements. When placing the components, the resistor and capacitor should be located as close to the MCU as possible.



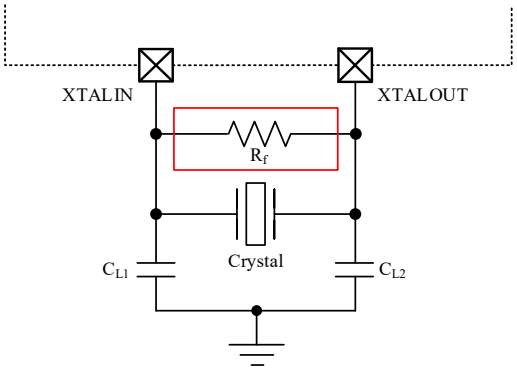
Clock

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, a clock prescaler, a clock multiplexer, an APB clock divider and a gating circuit. The clocks for the AHB, APB and Cortex®-M0+ are sourced from the system clock (CK_SYS) which can be sourced from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and the Real-Time Clock (RTC) use either the LSI or the LSE as their clock source.

The clock tree architecture can be obtained in the CKCU block diagram of the corresponding datasheet.

High Speed External Crystal Oscillator – HSE

The high speed external crystal oscillator, HSE, can provide a high accuracy clock source for the system clock. The relevant hardware design is shown below. The crystal, which has a specific frequency, must be connected between the two HSE pins (XTALIN / XTALOUT). The crystal should be located as close to the two HSE pins as possible. The supported frequency range of the crystal oscillator can be obtained from the high speed external clock characteristics in the datasheet. In order to ensure that the frequency oscillation reaches the nominal accuracy of the crystal oscillator, it is necessary to connect an external load capacitors C_L whose value can be obtained from the crystal oscillator datasheet. As some MCU types have no integrated feedback resistor, it might be necessary to connect an external feedback resistor. Refer to the CKCU section in the datasheet to check whether the device has an integrated feedback resistor.



The following guidelines are provided to improve the stability of the crystal circuit PCB layout.

- The crystal oscillator should be located as close as possible to the MCU so that the trace lengths are kept as short as possible to reduce any parasitic capacitances.
- Use a ground plane to shield any circuits near crystal to isolate signals and reduce noise.
- Keep frequently switching signal lines away from the crystal area to prevent crosstalk.

The HSE crystal oscillator can be switched on or off by using the HSEEN bit in the Global Clock Control Register (GCCR). The HSERDY flag in the Global Clock Status Register (GCSR) will indicate if the high speed external crystal oscillator is stable. When switching on the HSE, the HSE clock will not be released immediately for use until the HSERDY bit is set by the hardware. The specific delay period is well-known as “Start-up time”. As the HSE becomes stable, the HSE clock can then be used directly as the system clock source or as the PLL input clock.

The HSE clock monitor function is enabled by the HSE Clock Monitor Enable bit, CKMEN, in the Global Clock Control Register, GCCR. This function should be enabled after the HSE oscillator start-up delay and be disabled when the HSE oscillator is stopped. Once an HSE oscillator failure is detected, the HSE oscillator will be automatically disabled. The HSE Clock Stuck Flag, CKSF, in the Global Clock Interrupt Register, GCIR, will be set high. At this moment, if the clock fail interrupt enable bit, CKSIE, in the GCIR register is high, a clock failure interrupt is generated. This failure interrupt is connected to the CPU Non-Maskable Interrupt, NMI. If the HSE is directly used as the system clock, when an HSE oscillator failure occurs, the HSE will be turned off and the system clock will be switched to the HSI automatically by the hardware. If the HSE is used as the clock input of the PLL circuit and the system clock is sourced from the PLL circuit output, the PLL circuit and HSE will be turned off at the same time when the failure happens.

High Speed Internal Oscillator – HSI

The high speed internal RC oscillator, HSI, is the default clock source for the CPU when the device is powered on. The HSI RC oscillator provides a lower cost clock source because no external components are required. Compared with the external crystal oscillator, the HSI has a lower frequency accuracy. The HSI clock frequency and accuracy can be obtained from the HSI characteristics of the datasheet.

The HSI RC oscillator can be switched on or off by using the HSIEN bit in the Global Clock Control Register, GCCR. The HSIRDY flag in the Global Clock Status Register, GCSR, will indicate whether the internal RC oscillator is stable. The start-up time of the HSI is shorter than the HSE crystal oscillator. The HSI clock can also be used as the PLL input clock.

If the software configures the PSRCEN bit to 1, this will force the HSI clock to be the system clock when the device is woken up from the Deep-Sleep1 or Deep-Sleep2 mode. Subsequently, the system clock will be switched back to the original clock source, HSE or PLL, if the original clock source ready flag is set high. This function reduces the wakeup time when the HSE or the PLL is used as the system clock.

Auto Trimming the High Speed Internal Oscillator – HSI

The frequency accuracy of the high speed internal RC oscillator, HSI, can vary from one device to another due to manufacturing processes. This is the reason why each device still has a ±2 % accuracy at normal temperature and voltage after the calibration. For more information refer to the HSI characteristics in the datasheet. However, as this accuracy may not be good enough for some applications, the HT32 MCUs provide a trimming mechanism for the HSI frequency calibration using a more accurate external reference clock.

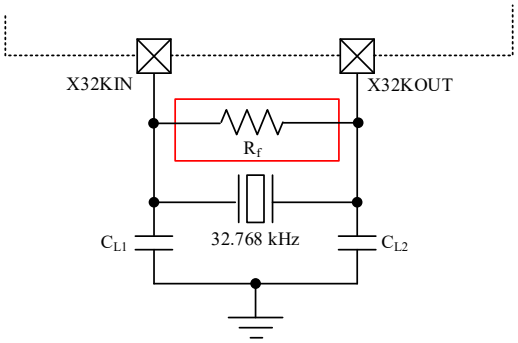
After a reset, the manufacturing trimming value is loaded into the HSICOARSE[4:0] and HSIFINE[7:0] bits in the HSI Control Register, HSICR. The HSI frequency accuracy is affected by voltage or temperature variations. If the application has to be driven by a more accurate HSI frequency, users can manually trim the HSI frequency using the HSIFINE[7:0] bits in the HSI Control Register, HSICR or automatically adjust the HSI frequency using the Auto Trimming Controller (ATC) together with an external reference clock. The reference clock can be sourced from the following clock sources.

- Low speed external crystal or ceramic resonator oscillator LSE with a frequency of 32768Hz
- 1kHz USB frame pulse
- External pin, CKIN, with a 1kHz pulse

Low Speed External Crystal Oscillator – LSE

The low speed external crystal or ceramic resonator oscillator has a 32768Hz frequency which produces a low power but highly accurate clock source for the Real-Time Clock circuit, Watchdog Timer or system clock. The relevant hardware configuration for this oscillator is shown below. The crystal or ceramic resonator must be placed near the two LSE pins, X32KIN and X32KOUT. In order to ensure that the oscillation frequency reaches the nominal accuracy of the crystal oscillator, it is necessary to connect an external load capacitors, C_L, whose value can be obtained from the crystal oscillator datasheet. As some MCU types do not have an integrated feedback resistor, it is necessary to connect an external feedback resistor. Refer to the CKCU section of the datasheet to check whether the device has an integrated feedback resistor.

The LSE oscillator can be switched on or off by using the LSEEN bit in the RTC Control Register, RTCCR. The LSERDY flag in the Global Clock Status Register, GCSR, will indicate if the LSE clock is stable.



Low Speed Internal RC Oscillator – LSI

The low speed internal RC oscillator has a frequency of about 32kHz and is a low power clock source for the Real-Time Clock circuit, Watchdog Timer or system clock. It is a low cost clock source which does not require external components. The frequency accuracy of the low speed internal RC oscillator can be obtained from the corresponding datasheet.

Phase Lock Loop – PLL

The PLL is a phase lock loop frequency multiplier whose clock input source can be sourced from the HSI or the HSE. The input frequency can be multiplied to the target frequency by configuring the relevant configuration registers. The configuration method can be obtained from the CKCU section of the corresponding datasheet. Its electrical characteristics can be obtained from the corresponding datasheet.

USB Phase Lock Loop – USB PLL

This USB PLL can provide a USB peripheral clock with 48MHz which is 3~12 times the fundamental reference frequency of 4~16MHz. The rationale of the clock synthesizer relies on a digital Phase Lock Loop, which includes a reference divider, a two-stage feedback divider, a two-stage output divider, a digital phase frequency detector, PFD, a current-controlled charge pump, a built-in loop filter and a voltage-controlled oscillator, VCO, to achieve a stable phase-locked state.

Boot Configuration

The system provides three kinds of boot modes including the bootloader, main Flash and SRAM, which can be selected through the BOOT pin. The BOOT pin has an internal pull-up resistor with an enable control. The number of BOOT pins and the boot modes vary with the different MCU types. The M0+ series only has a single boot pin, therefore users can select either the bootloader mode or the main Flash mode. The M3 series has two boot pins, BOOT0 and BOOT1, which provide three boot modes for user selection. Refer to the datasheet for the detailed mode information.

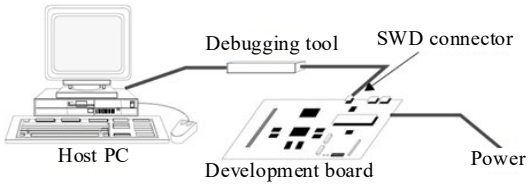
The BOOT pin status is sampled during a power-on reset or a system reset. Once the logic value on these pins has been determined, the first 4 words of the vector will be remapped to the corresponding source according to the boot mode.

Debug Management

The host/target interface is composed of hardware connecting the host PC to the application circuit board. This interface consists of three parts, a hardware debug tool, an SWD connector and a cable which connects the host PC to the debugging tool.

The connection between the host PC and the development board is shown below.

The debug tool, e-Link32 Lite, has been embedded into the HT32 development board, therefore the development board can be connected to the PC directly using a USB cable.



SWD Port - Serial Wire Debug

The HT32 series core includes an integrated Serial Wire Debug Port (SW-DP) interface. This port is an Arm® standard CoreSight™ debug port with two pins, which are clock and data pins.

Pins and Debug Port Pins

The number of the available pins varies with different HT32 MCU packages. Refer to the pin assignment diagram in the corresponding datasheet for more detailed information.

1. Serial Wire Debug, SWD, pin assignment

   The SWD pin assignment of most HT32 packages are the same.

SWD Pin Name	SWD Port		Pin Assignment
	Type	Debug Assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA12

2. SWD pin assignment

   After a reset (SYSRESETn or PORESETn), these pins will be assigned as the dedicated pins immediately for use by the host PC which runs the debug software.

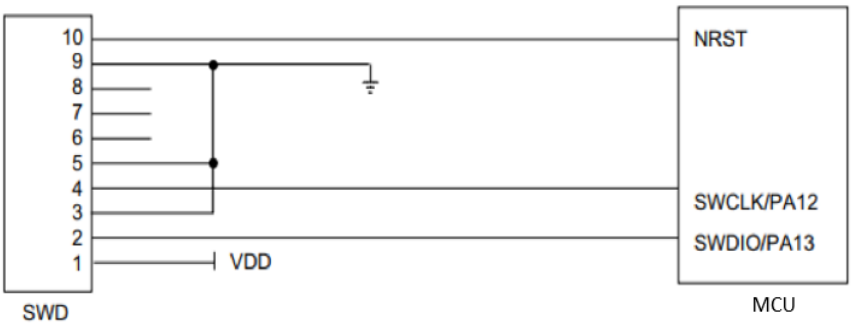
   The MCU can use the SWD pins as General-Purpose Input/Output (GPIO) pins. Refer to the GPIO and AFIO sections in the corresponding datasheet for more detailed information.

3. SWD pins internal pull-up and pull-down resistors

   If the user software has released the SWD I/O functions, the GPIO controller will take charge of these pins. These two I/O pins will then be set to the status equivalent of the reset status of the relevant GPIO control register.

   - SWDIO: Input enable with internal pull-up
   - SWCLK: Input enable with internal pull-up

As there are internal pull-up resistors, no external resistor is required.



Recommendations for Hardware PCB Layout

Printed Circuit Board

For technical reasons, it is preferable to use multilayer printed circuit boards (PCB), one layer of which should be dedicated for use as a ground plane, V_{SS}, and another dedicated for use as a power plane, V_{DD}. In this way, better decoupling and shielding effects can be implemented. For many applications, this kind of PCB cannot be used due to cost considerations. For these applications, the main requirement will be to ensure that the grounding structure and the power structure are good.

Component Position

The initial PCB traces should include the following separated circuits.

- High current circuits
- Low voltage circuits
- Digital component circuits

Due to the influence of EMI, circuits should adopt the independent traces, which reduces cross coupling on the PCB and reduces noise.

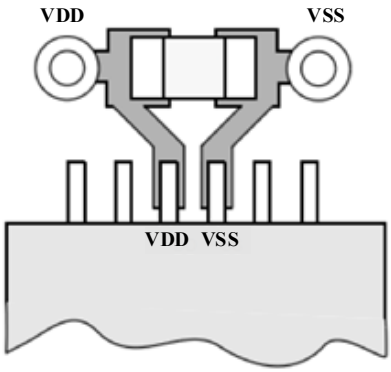
Grounding and Power - VSS, VDD, VDDA

Every section for either noise, whether it is low voltage sensitive or digital should be connected to ground independently and all the ground loops should be connected. It is necessary to avoid loops and minimise any areas of influence. In order to improve analog performance, it is recommended

to use independent power lines for V_{DD} and V_{DDA} and place decoupling capacitors as close to the components as possible. The power lines should be close to the ground line to minimise any power loop areas. This is because power loops can actually act as an antenna, which will become a primary EMI transmitter and receiver. All PCB areas without components must be covered with additional ground lines to implement a certain shielding effect especially when using single layer PCBs.

Decoupling

All the power and ground pins must be correctly connected to the power properly. The impedance of these connection lines, including pads, routings and vias, must be as low as possible. This can usually be implemented by increasing the route width, preferably using a dedicated power plane if using multi-layer PCBs. In addition, a 100nF filter ceramic capacitor and an electrolytic capacitor of about 4.7μF are connected between the VDD and VSS pins for decoupling. These capacitors should be placed as close as possible to or below the corresponding pins on the lower side of the PCB. The typical value of a filter ceramic capacitance should be in a range of 10nF to 100nF, but the specific value depends on the actual application requirements. The following diagram shows typical routing for the VDD and VSS.



Considerations

BOOT Pin Consideration

The boot mode is selected by the BOOT pins. During an MCU reset, the BOOT pin status is sampled to determine whether the program starts from the Main Flash, the ISP BootLoader or the SRAM. It should be noted that only the MCUs with both BOOT0 and BOOT1 pins have the SRAM boot mode. MCUs with only one BOOT pin only have two boot modes, Main Flash and ISP BootLoader.

BOOT pin functional description:

1. The pin status of BOOT or BOOT1 during a reset.

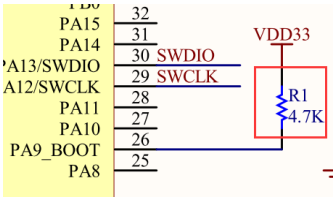
   Logic 1: The MCU boots from the Main Flash.

   Logic 0: The MCU boots from the ISP BootLoader or the SRAM

2. After a reset, the internal pull-up resistor on the BOOT pin will be enabled by default. Here the resistor value is about 46kΩ. Refer to the datasheet for the specific value.

   Based on the above two points, the following notes should be considered:

   - If the BOOT pin is not pin-shared with other functions, it can be left unconnected. However, it is recommended to externally connect it to a resistor to reduce any ESD/EFT influences.
   - The BOOT pin can be used as an output pin. Considering that a WDT Reset or an NVIC Reset executes rapidly, the BOOT pin voltage rise rate may be insufficient if it is only relying on the internal pull-up resistor. In order to prevent the MCU from entering the ISP BootLoader or SRAM by mistake, an external 4.7kΩ pull-up resistor connected to the MCU's VDD pin should be connected.



   - The BOOT pin should not be used as an input unless it is certain that the BOOT or BOOT1 pin will have a logic "1" condition after a reset.

Layout Consideration

- Avoid placing power lines beneath the MCU. Additionally, DGND and the high frequency output lines should retain a certain distance from each other and not be parallel to each other to avoid coupling interference. Also high current power lines should be kept at a certain distance from both the MCUs DGND and VDD lines to avoid coupling interference.
- The power lines should not be routed on the edge of the PCB to avoid EMI influence.
- A magnetic bead should be added between the digital power and the analog power lines for isolation purposes.

Conclusion

For designers who are using the HT32 MCUs for the first time, this application note can assist them to more rapidly design safe and stable hardware requiring reduced revisions.

Reference Material

For more information, refer to the Holtek official website: http://www.holtek.com.

Revision and Modification Information

Data	Author	Issue	Modification Information
2022.9.26	李承锴	V1.00	First Version

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