

HT32 Series Microcontroller Flash Programming

D/N: AN0465E

Overview

This manual describes the methods for programming the HT32 series. The supported MCUs are the Holtek 32-bit devices that include the Cortex-M0+ or Cortex-M3 processor.

The HT32 series devices embedded Flash can be programmed in several ways such as using In-System Programming (ISP), In-Application Programming (IAP) or In-Circuit Programming (ICP).

While the application is running, IAP is an important method for Flash Memory programming. This can be used for firmware upgrades using specific communication types such as USB, USART, I2C Slave Mode and SPI Slave Mode, etc. If the IAP programming method is used, the Flash main block will be divided into two blocks, namely IAP and AP. The IAP block is used to update the AP block contents. The IAP block firmware must be first pre-programmed into the Flash using an ICP or Writer.

ISP is similar to IAP for updating the Flash memory except that it is located in the Bootloader which is programmed by Holtek using the USART or USB as the communication protocol. The Bootloader is pre-programmed into the Flash information block before the MCU is produced and after programming they cannot be changed by the application.

The in-circuit programming (ICP) method is used to download the complete Flash memory data. Both the Joint Test Action Group (JTAG) and Serial Wire Debug (SWD) interfaces can be used to load the program data into the Flash main block.

The in-circuit programming (ICP) method function does not require the MCU Flash internal firmware to be running as the MCU is programmed using the integration development environment along with the ICE. The devices are well supported by professional IDE suppliers including IAR EWARM and Keil MDK-ARM. In addition, Holtek provides its own e-Link32 Pro which provides offline programming which is another in-circuit programming (ICP) method.

The Flash interface performs instruction access and data access via the Cortex-M0+/M3 core bus. A pre-fetch buffer is used to reduce instruction gaps. The Flash operations include Program, Page Erase and Mass Erase and also Read/Write protection functions.

Features

- 1 KB or 512-byte Page size (Refer to the User Manual FMC section for more page size details)
- Wide read interface and a pre-fetch buffer are used to reduce instruction gaps
- Flash program / page erase / mass erase capability
- Flash read protection to prevent illegal code / data access
- Page erase / program protection to prevent unexpected operation

Flash Memory Architecture

The Flash memory consists of a main block and an information block. The main block contains multiple pages of 1 KB or 512-byte each. Refer to Table 1 and Table 2 for details.

The Flash memory is implemented using 32-bit words for both instruction and data storage. The Flash memory is configured according to the memory capacity of the Holtek 32-bit devices that include the Cortex-M processor. The Flash memory is located at the specific addresses in the HT32 series devices memory map, with a base address of 0x00000000.

The main block write operation is controlled by the Flash Memory Controller, otherwise known as the FMC. The FMC manages the program and erase procedures.

The information block is reserved for the Bootloader which is then used as an ISP to re-program the main block using the USART or USB interfaces. The device can be booted in the Bootloader mode if the BOOT pin is pulled low.

The Flash memory can also be protected against any unexpected read / write / page erase operations. Refer to Section 2.4 for more details.

During write or erase operations, read operations cannot be executed. The High Speed Internal RC Oscillator, HIS, must be enabled before any write/erase operations are executed.

Table 1 Flash Memory Architecture - using the HT32F52352 as an example

Block type	Name	Address	Page Protection Bit	Size
Main Block	Page 0	0x0000_0000 ~ 0x0000_01FF	OB_PP [0]	512-byte
	Page 1	0x0000_0200 ~ 0x0000_03FF	OB_PP [0]	512-byte
	Page 2	0x0000_0400 ~ 0x0000_05FF	OB_PP [1]	512-byte
	Page 3	0x0000_0600 ~ 0x0000_07FF	OB_PP [1]	512-byte
	:	:	:	:
	:	:	:	:
	Page 252	0x0001_F800 ~ 0x0001_F9FF	OB_PP [126]	512-byte
	Page 253	0x0001_FA00 ~ 0x0001_FBFF	OB_PP [126]	512-byte
	Page 254	0x0001_FC00 ~ 0x0001_FDFF	OB_PP [127]	512-byte
	Option Byte	Physical: 0x0001_FE00 ~ 0x0001_FFFF Alias: 0x1FF0_0000 ~ 0x1FF0_01FF	OB_CP [1]	512-byte
Information Block	Boot Loader	0x1FF0_0000 ~ 0x1FF0_0FFF	NA	4 KB

Table 2 Flash Memory Architecture - using the HT32F12366 as an example

Block type	Name	Address	Page Protection Bit	Size
Main Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1 KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [0]	1 KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [1]	1 KB
	Page 3	0x0000_0C00 ~ 0x0000_0FFF	OB_PP [1]	1 KB
	:	:	:	:
	:	:	:	:
	Page 252	0x0003_F000 ~ 0x0003_F3FF	OB_PP [126]	1 KB
	Page 253	0x0003_F400 ~ 0x0003_F7FF	OB_PP [126]	1 KB
	Page 254	0x0001_F800 ~ 0x0003_FBFF	OB_PP [127]	1 KB
	Option Byte	Physical: 0x0003_FC00 ~ 0x0003_FFFF Alias: 0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1 KB
Information Block	Boot Loader	0x1F00_0000 ~ 0x1FF0_1FFF	NA	8 KB

HT32 Series Devices Embedded Flash Operations

Read Operation

The embedded Flash memory is just like any other common memory in that it can be addressed directly. The access interface reads from the Flash memory and stores the instruction/data in the pre-fetch buffer. The pre-fetch buffer can be disabled if the enable bit, PFBE, in the Flash pre-fetch control register is reset. By default, the pre-fetch buffer will be on.

Program/Erase Operation

The Flash Memory Controller (FMC) provides the Flash memory program and erase functions.

Flash Programming

The FMC provides a 32-bit word programming function to write to the Flash memory. The following steps show the word programming operation register access sequence.

1. Check the OPCR register to confirm that no Flash memory operations are in progress (OPM [3:0] is equal to 0xE or 0x6). Otherwise, wait until the previous operation has finished.
2. Write the word address into the TADR register.
3. Write the word data into the WRDR register.
4. Write the word program command into the OCMR register (CMD [3:0] = 0x4).
5. Send the word program command to the FMC by setting the OPCR register (set OPM [3:0] equal to 0xA).
6. Wait until all operations have finished by checking the value of the OPCR register (OPM [3:0] = 0xE).

7. Read and verify the Flash memory if required, which is implemented by accessing the Cortex-M0+/M3 core bus.

Note: the Flash word programming operation cannot be applied to the same address twice. Successive word programming operations to the same address must be separated by a page erase operation. Additionally, the word program operation will be ignored on write protected pages. A Flash operation error interrupt will be triggered when the OREIEN bit in the OIER register is set. Check the PPEF bit in the OISR register to detect this condition in the interrupt handler.

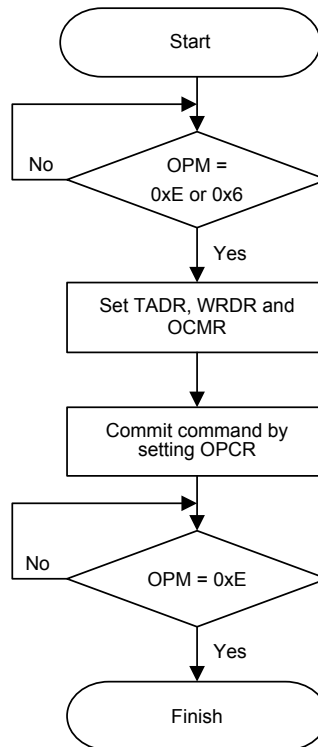


Figure 1 Flash Word Programming Flowchart

Page Erase

The FMC provides a page erase function which is used to erase the contents of a specific Flash page. Each page can be erased independently. The following steps show the page erase sequence.

1. Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] is equal to 0xE or 0x6). Otherwise, wait until the previous operation has finished.
2. Write the page address into the TADR register.
3. Write the page erase command into the OCMR register (CMD [3:0] = 0x8).
4. Send the word program command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA)
5. Wait until all operations have finished which can be done by checking the value of the OPCR register (OPM [3:0] is equal to 0xE).
6. Read and verify the Option Byte if required, which is implemented by accessing the Cortex-M0+/M3 core bus.

The correct address of the targeted page must be confirmed. The software may run out of control if the targeted erase page is being used for code or data fetching. Note that the page erase operation will skip over the write protected pages. A Flash operation error interrupt will be triggered when the OREIEN bit in the OIER register is set. Check the PPEF bit in the OISR register to detect this condition in the interrupt handler.

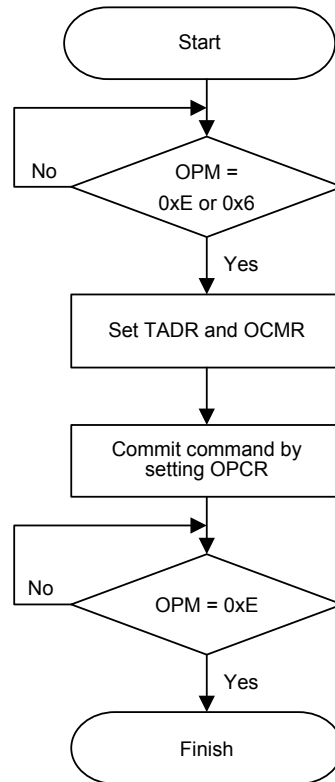


Figure 2 Flash Page Erase Flowchart

Mass Erase

The FMC provides a mass erase function which is used to erase all pages in the main block. The following steps show the mass erase operation sequence.

1. Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] is equal to 0xE or 0x6). Otherwise, wait until the previous operation has finished.
2. Write the mass erase command to the OCMR register (CMD [3:0] = 0xA).
3. Send the mass erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
4. Wait until all operations have completed by checking the value of the OPCR register (OPM [3:0] is equal to 0xE).
5. Read and verify the Flash memory if required, which is implemented by accessing Cortex-M0+/M3 core bus.

When the mass erase operation has finished, the main block will be erased to 0xFFFF_FFFF. The mass erase operation can be implemented by an application that runs in the SRAM or by the debug tool.

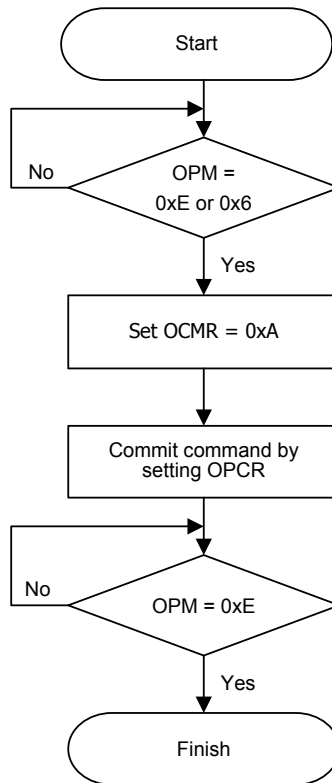


Figure 3 Flash Mass Erase Flowchart

Option Byte Block

The Option Byte can be treated as an independent Flash memory whose base address is 0x1FF0_0000. The option bytes consist of 6 words that are used for Flash read/write protection functions.

After a reset, the option bytes will be reloaded and their contents will be stored into the FMC registers. If the checksum of the option byte is incorrect, a checksum error will occur with the OBEF bit in the OISR register being set high. The Flash read/write protection function will be enabled to prevent an illegal access.

Table 4 Option Byte Organisation

Option Byte	Offset	Description	Reset Value
Option Byte Base Address = 0x1FF0_0000			
OB_PP	0x000	OB_PP [n]: Flash Page Erase / program Protection (n = 0 ~ 30 for page 0 ~ page 30)	0xFFFF_FFFF
	0x004		0xFFFF_FFFF
	0x008	0: Enable	0xFFFF_FFFF
	0x00C	1: Disable	0xFFFF_FFFF
		OB_PP [127:31]: Reserved	
OB_CP		OB_CP [0]: Flash Security Protection	0xFFFF_FFFF
		0: Enable	
		1: Disable	
	0x010	OB_CP [1]: Option Byte Protection	
		0: Enable	
		1: Disable	
		OB_CP [31:2]: Reserved	

Option Byte	Offset	Description	Reset Value
OB_CK	0x020	OB_CK [31:0]: Flash Option Byte Checksum OB_CK should be set as the sum of 5 words Option Byte content, of which the offset address ranges from 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the OB_PP or OB_CP register content is not equal to 0xFFFF_FFFF.	0xFFFF_FFFF

Flash Protection

The main block of the Flash memory can be protected to prevent illegal accesses from untrusted code. The pages of the main block can also be protected independently to prevent any unexpected write operations.

- Security Protection

This function is useful to provide protection from illegal users. The function is activated by configuring the OB_CP [0] bit in the Option Byte. Once the function has been enabled, page 0 and the Option Byte block are write-protected automatically. All Flash bus accesses, program and page erase operations will not be allowed in the debug mode. However, the mass erase operation will still be accepted by the FMC in order to disable this security protection function.

- To enable the security protection, the procedure below should be followed.
 1. Program the OB_CP [0] as 0.
 2. OB_CK should be set as the sum of 5 words Option Byte content that is addressed from 0x0~0x13.
 3. Generate a system reset to activate the new OB_CP setting.
- To disable the security protection, the procedure below should be followed.
 1. Perform a mass erase. At this point note that the security protection is still enabled.
 2. Generate a power-on reset to activate the new OB_CP setting.

- Write Protection

Write protection can be individually enabled by setting OB_PP for each page of the main block. If a page erase/program operation is performed on a protected page, the PPEF bit in the OISR register will be set. If the OREIEN bit in the OIER register is also set, a Flash operation error interrupt will be triggered by the FMC.

If a page erase operation is performed on an option byte block, all write protection functions will be disabled. The write protection of the option byte region is activated by clearing OB_CP [1] to 0. If the option byte block has been protected, the only way to disable the write protection is to execute a mass erase operation.

- To enable the write protection, the procedure below should be followed.
 1. Program the OB_PP [m:n] to 0 to enable protection of the corresponding page.
Program the OB_CP [1] to 0 to enable protection of the option byte block.
 2. Program the OB_CK as the sum of the 5 word option byte content that is addressed from 0x0~0x13
 3. Generate a system reset to activate the new OB_PP/OB_CP setting.
- To disable the main block pages write protection, the procedure below should be followed.
 1. Erase the option byte block when the Option Byte page protection is disabled
 2. Generate a system reset to activate the new OB_PP setting.

- To disable the write protection of option byte block, the procedure below should be followed.
 1. Perform a mass erase.
 2. Generate a system reset to activate the new OB_CP setting.

Register Description

The following table shows the FMC registers and reset values.

Table 5 FMC Register Map

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt and Status Register	0x0001_0000
PPSR	0x020	Flash Page Erase / program Protection Status Register	0XXXXX_XXXX
	0x024		0XXXXX_XXXX
	0x028		0XXXXX_XXXX
	0x02C		0XXXXX_XXXX
CPSR	0x030	Flash Security Protection Status Register	0x0000_000X
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X

Note: "X" means various reset values which depend on the Device, Flash value, option byte value, or power on reset setting.

Flash Target Address Register – TADR

This register specifies the target address of the page erase and word programming operations.

Offset:	0x000							
Reset value:	0x0000_0000							
	31	30	29	28	27	26	25	24
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	23	22	21	20	19	18	17	16
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	15	14	13	12	11	10	9	8
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	7	6	5	4	3	2	1	0
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0

Bits	Field	Descriptions
[31:0]	TADB	<p>Flash Target Address Bits</p> <p>For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32-bits, the TADR should be set as word-aligned (4-byte). The TADB [1:0] will be ignored during programming operations.</p> <p>For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1KB or 512-byte, some TADB bits will be ignored in order to limit the target address as 1 KB-aligned or 512-byte alignment.</p> <p>This field is used to specify the Flash address which must be within the range from 0x0000_0000 to 0x1FFF_FFFF. Otherwise, an Invalid Target Address interrupt will be generated if the corresponding interrupt enable bit is set.</p>

Flash Write Data Register – WRDR

This register stores the data to be written into the TADR register for programming operations.

Offset: 0x004
 Reset value: 0x0000_0000

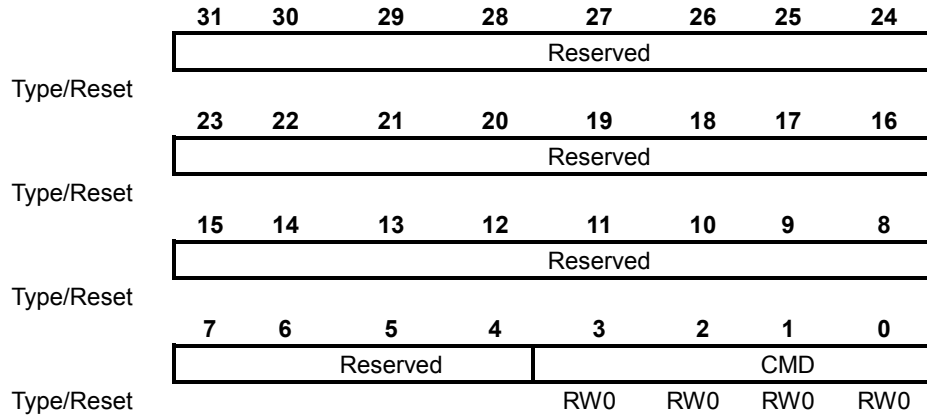
	31	30	29	28	27	26	25	24
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	23	22	21	20	19	18	17	16
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	15	14	13	12	11	10	9	8
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	7	6	5	4	3	2	1	0
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0

Bits	Field	Descriptions
[31:0]	WRDB	<p>Flash Write Data Bits</p> <p>The data value for programming operation.</p>

Flash Operation Command Register – OCMR

This register is used to specify the Flash operation commands that include word programming, page erase and mass erase.

Offset: 0x00C
 Reset value: 0x0000_0000



Bits	Field	Descriptions
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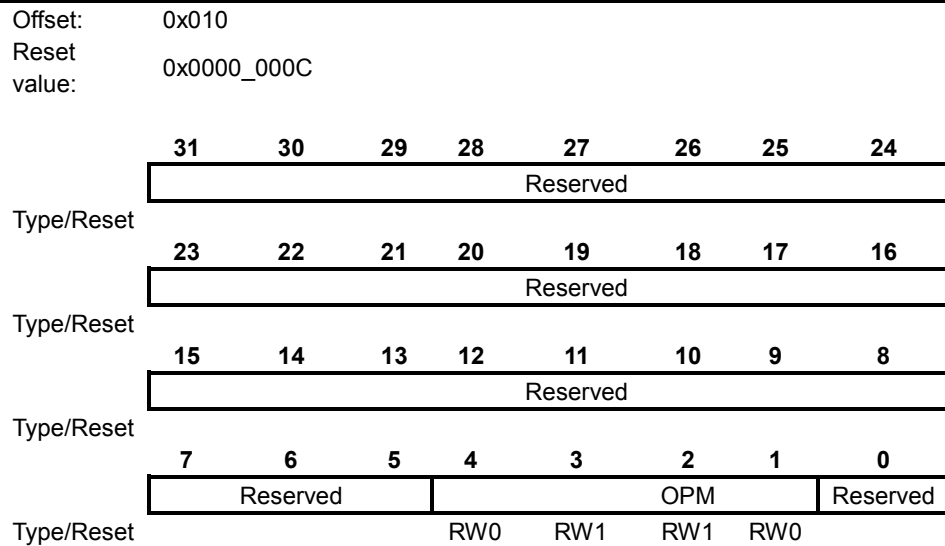
[3:0]	CMD	Flash Operation Command
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The following table shows the operation command bits CMD [3:0] definitions which determine the Flash memory operation. If an invalid command is set and the IOCMIE bit is equal to 1, an Invalid Operation Command interrupt will be generated.

CMD [3:0]	Description
0x0	Idle – default
0x4	Word program
0x8	Page erase
0xA	Mass erase
Others	Reserved

Flash Operation Control Register – OPCR

This register is used for controlling the command commitment and checking the status of the FMC operations.



Bits	Field	Descriptions
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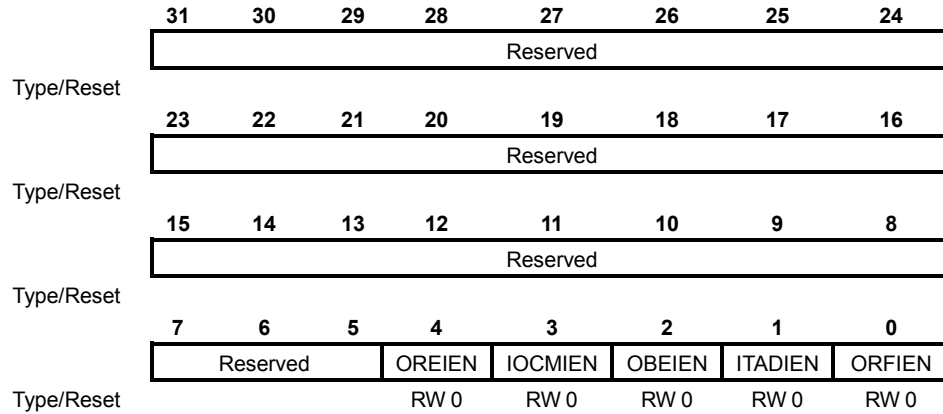
[4:1]	OPM	<p>Operation Mode</p> <p>The following table shows the operation modes of the FMC. Users can commit the command which is set by the OCMR register for the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR and OCMR registers should be prepared before setting this register. After all the operations have finished, the OPM field will be set as 0xE or 0xF by the FMC hardware. The Idle mode can be set when all the operations have been finished for power saving. Note that the operation status should be checked before the next operation is executed on the FMC. The content of the TADR, WRDR, OCMR and OPCR registers should not be changed until the previous operation has finished.</p>
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OPM [3:0]	Description
0x6	Idle - default
0xA	Commit command to main Flash
0xE	All operation finished on main Flash
Others	Reserved

Flash Operation Interrupt Enable Register – OIER

This register is used to enable or disable the FMC interrupt function. The FMC generates an interrupt to the controller when the corresponding interrupt enable bits are set.

Offset: 0x014
 Reset value: 0x0000_0000



Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Disable 1: Enable
[3]	IOCM IEN	Invalid Operation Command Interrupt Enable 0: Disable 1: Enable
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Disable 1: Enable
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Disable 1: Enable
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Disable 1: Enable

Flash Operation Interrupt and Status Register – OISR

This register indicates the status which is used to check if an operation has finished or if an error has occurred. The status bits are available when the corresponding bits in the OIER register are set.

Offset:	0x018																
Reset value:	0x0001_0000																
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7	6	5	4	3	2	1	0										
Reserved			OREF	IOCMF	OBEF	ITADF	ORFF										
Type/Reset	WC0 WC0 WC0 WC0 WC0																

Bits	Field	Descriptions
[17]	PPEF	Page Erase / Program Protected Error Flag 0: Page Erase / Program Protected Error does not occur 1: Operation error has occurred due to an invalid page erase / program operation being applied to a protected page This bit is reset by hardware once a new Flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last flash operation command is has not yet finished 1: The last flash operation command has finished This bit is directly connected to the Flash memory for debugging purposes.
[4]	OREF	Operation Error Flag 0: No flash operation error occurred 1: The previous flash operation has failed This bit will be set when any Flash operation error has occurred such as an invalid command, program error and erase error, etc. occurs. The ORE interrupt occurs if the OREIEN bit in the OIER register is set. This bit will be reset by software.
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid flash operation command was set 1: An invalid flash operation command has been set into the OCMR register An IOCM interrupt will occur if the IOCMIEN bit in the OIER register is set. This bit will be reset by software.
[2]	OBEF	Option Byte Check Sum Error Flag 0: Option Byte checksum is correct 1: Option Byte checksum is incorrect An OBE interrupt will occur if the OBEIEN bit in the OIER register is set. This bit will be reset by software.

Bits	Field	Descriptions
[1]	ITADF	Invalid Target Address Flag 0: The target address is valid 1: The target address TADR is invalid The data in the TADR field must be within the range from 0x0000_0000 to 0x1FFF_FFFF. An ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. This bit will be reset by software.
[0]	ORFF	Operation Finished Flag 0: No operation finished interrupt occurred 1: Previous flash operation command has finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. This bit will be reset by software.

Flash 1 Page Erase / program Protection Status Register – PPSR

This register indicates the page erase / program protection status of the Flash memory.

Offset: 0x020 (0) ~ 0x02C (3)
Reset value: 0xFFFF_XXXX

	31	30	29	28	27	26	25	24
	PPSBn							
Type/Reset	ROX	ROX	ROX	ROX	ROX	ROX	ROX	ROX
	23	22	21	20	19	18	17	16
	PPSBn							
Type/Reset	ROX	ROX	ROX	ROX	ROX	ROX	ROX	ROX
	15	14	13	12	11	10	9	8
	PPSBn							
Type/Reset	ROX	ROX	ROX	ROX	ROX	ROX	ROX	ROX
	7	6	5	4	3	2	1	0
	PPSBn							
Type/Reset	ROX	ROX	ROX	ROX	ROX	ROX	ROX	ROX

Bits	Field	Descriptions
[127:0]	PPSBn	Page n Erase / program Protection Status Bits (n = 0 ~ 127) PPSB[n] = OB_PP[n] 0: The corresponding pages are protected 1: The corresponding pages are not protected The contents of this register are not dynamically updated and will only be reloaded from the Option Byte when any kind of reset occurs. The erase or program function of the specific pages is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of PPSR [127:0] is determined by the Option Byte OB_PP [127:0] bits. The total number of flash memory pages for the HT32 series devices will be different because of the different device specifications. Therefore, only the OB_PP [n:0] and PPSR [n:0] bits are valid (where n = chip flash page number - 1). The other bits of the OB_PP and PPSR registers are reserved for future usage.

Flash Security Protection Status Register – CPSR

This register indicates the Flash memory security protection status. The contents of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is active when any kind of reset occurs.

Offset:	0x030
Reset value:	0x0000_000X
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 3130292827262524 </div>	
Type/Reset	Reserved
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 2322212019181716 </div>	
Type/Reset	Reserved
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 15141312111098 </div>	
Type/Reset	Reserved
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 76543210 </div>	
Type/Reset	<div style="flex-grow: 1; text-align: center;">Reserved</div> <div style="text-align: center;">OBPSB</div> <div style="text-align: center;">CPSB</div>
	ROX ROX

Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase / program Protection Status Bit 0: The Option Byte page is protected 1: The Option Byte page is not protected The reset value of OPBSB is determined by the Option Byte OB_CP [1] bit.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Security protection is enabled 1: Flash Security protection is not enabled The reset value of CPSB is determined by the Option Byte OB_CP [0] bit.

Versions and Modify Information

Date	Author	Issue and Revision
2017.10.25	Michael, Wu	First Version

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