HT32 Series Crystal Oscillator, ADC Design Note and PCB Layout Guide

D/N：AN0301E

Introduction

This application note provides some hardware design notes for the Crystal Oscillator and the Analog to Digital Converter in the Holtek 32-bit MCU HT32 series. The Crystal Oscillator architecture type is a Pierce oscillator and the ADC is based on a SAR structure. PCB layout guidelines are additionally provided.

Crystal Oscillator

The HT32 series devices have four types of oscillators, these are the High Speed Internal RC oscillator (HSI), the High Speed External crystal oscillator (HSE), the Low Speed Internal RC oscillator (LSI) and the Low Speed External crystal oscillator (LSE). This chapter introduces the crystal oscillator for both the HSE and LSE.

Crystal Equivalent Circuit

Figure 1 shows a conventional equivalent circuit of a crystal at a frequency near its main resonant frequency. The components, L_{qz}, C_s, and R_{qz} are known as the motional parameters of the crystal. The component C_p represents the shunt capacitance resulting from stray capacitance between the crystal electrodes.

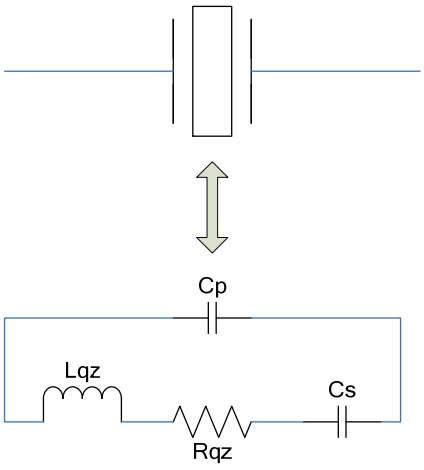

Figure 1 Crystal Equivalent Circuit

Table 1 gives examples of component values for a nominal crystal frequency of 8MHz.

Equivalent Component	Value
L_{qz}	24.38mH
C_s	0.016pF
R_{qz}	50Ω
C_p	5pF

Table 1 8MHz Crystal Equivalent Component Values

HT32 Series Pierce Oscillator

The Pierce oscillator architecture is shown in Figure 2. It is used for the HT32 internal oscillator circuit due to its low power consumption, low cost and stability.

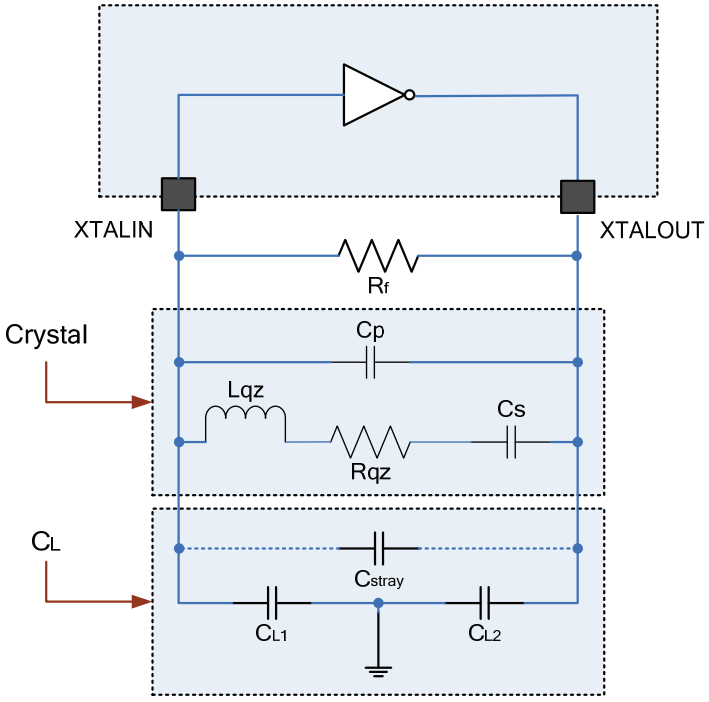

Figure 2 Pierce Oscillator Architecture

HT32 Series Crystal Oscillator Application Circuit

Figure 3 shows the Pierce oscillator circuit in the HT32 series. The following section will assist with the calculation of suitable external load capacitors.

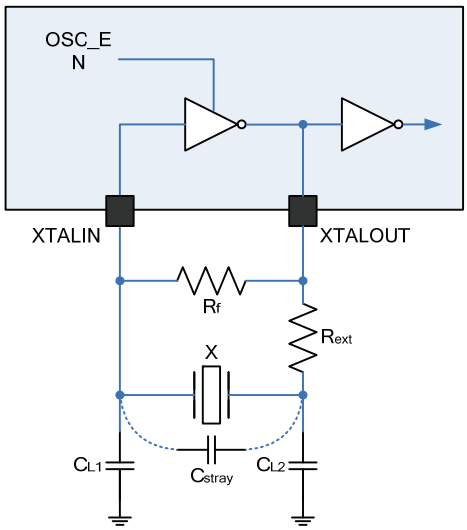

Figure 3 HT32 Series Crystal Oscillator Circuit

Figure 3 Parameter Description

X: Quartz crystal or ceramic resonator

R_f: External feedback resistor

R_{ext}: External resistor to limit the inverter output current

C_{L1} and C_{L2}: External load capacitors.

C_{stray}: Printed circuit board and external connection stray capacitance – parasitic capacitance.

- R_f represents the feedback resistor to bias the inverter in the high gain region. R_f cannot be too low otherwise the loop may fail to oscillate. In the HT32 series MCUs, a 1MΩ is used for a 8MHz HSE and 10MΩ is used for the 32,768Hz LSE.
- R_{ext} represents the damping resistor that helps increase stability, saves power, and suppresses gain in the high frequency area. The trade-off for inserting R_{ext} is the reduction of negative resistance. Therefore, R_{ext} cannot be too large; otherwise the loop may fail to oscillate. Sometimes R_{ext} may be omitted for high frequency oscillation applications to reduce production costs.
- The values of the external capacitors C_{L1} and C_{L2} are determined according to the crystal or ceramic resonator load capacitance C_L specification as provided by the manufacturer. These two external capacitors are used to provide small frequency adjustments. The crystal or ceramic resonator manufacturer needs to provide the C_L value. For steady state oscillation, the load capacitance C_L is given by:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_{stray}$$

It must be noted that the device I/O ports, bond pads, package pins and the printed circuit board will all contribute to the value of the parasitic capacitance, Cstray, which will compose the load capacitance C_L. Therefore, the required external load capacitors, C_{L1} and C_{L2} of the crystal or ceramic resonator, will be reduced in value.

C_{L1} and C_{L2} Example Calculation

If the crystal C_L value is equal to 20pF and assuming that Cstray = 5pF, then:

$$C_L - C_{stray} = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = 10\,pF - 5pF = 5pF$$

Therefore:

$$C_{L1} = C_{L2} = 10pF$$

Crystal Circuit PCB Layout Guidelines

The following guidelines are provided to improve the stability of the crystal circuit PCB layout.

- The crystal oscillator should be located as close as possible to the MCU so that the trace lengths are kept as short as possible to reduce any parasitic capacitances.
- Shield any lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
- Keep frequently switching signal lines away from the crystal area to prevent crosstalk.

ADC - Analog to Digital Converter

The HT32 series 12-bit ADC is based on a successive approximation, SAR, structure due to its low power, high performance and small form factor. The ADC has multiplexed input channels including multiple external channels on which the external analog signals can be measured, and 2 internal channels (V_{REF-}, V_{REF+}). Refer to the corresponding data sheet for mote details regarding the ADC channel numbers. The ADC can be operated in single shot, continuous and discontinuous conversion modes.

The ADC and digital domains are separated inside the chip with different power supplies (V_{DDA}, V_{DD33}). The ADC reference voltage, V_{REF} and V_{REF+}, are internally bonded together with the ADC ground (V_{SSA}) and power supply (V_{DDA}) for the HT32 series MCUs. This means that when V_{DDA} equals 3.3V, then the resolution is 3.3V / 4096 = ~0.8mV/bit. In order to obtain higher resolutions, low voltage noise suppression on the V_{SSA} ground and V_{DDA} supply power lines are important considerations. To suppress noise on the device supply power supply, proper decoupling capacitors on the PCB are very important.

Improving the ADC Accuracy

Figure 4 shows the equivalent circuit of the S/H input stage of the HT32 series SAR ADC, where C_I is the internal storage capacitor, R_I is the resistance of the internal sampling switch and R_S is the output impedance of the signal source V_S. In normal cases, the duration of the sampling phase is approximately $1.5/f_{ADC}$. C_I must be charged during this phase, and it must be ensured that the voltage on its terminals becomes sufficiently close to V_S. To guarantee this, R_S may not have an arbitrarily large value.

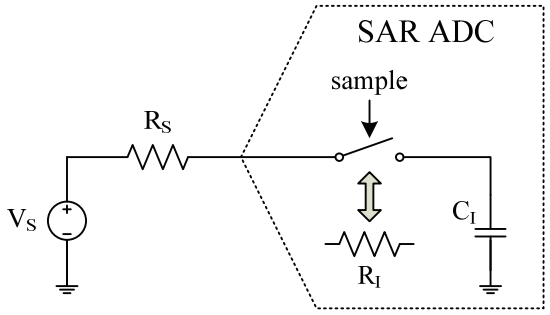

Figure 4 ADC Sampling Network Model

The worst case occurs when the extremities of the input range (V_{REF-} and V_{REF+}) are sampled consecutively. In this situation, a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{1.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Here f_{ADC} is the ADC clock frequency and N is the ADC resolution (N=12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model. If, in the system where this ADC is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated in the equation above.

Example of R_S Calculation

If the C_I and R_I value of the ADC obtained from the data sheet are equal to 5pF and 1kΩ, and assuming that the ADC clock frequency is 14MHz (1Msps), the ADC has 12-bit resolution and the duration of the sampling phase is $1.5/f_{ADC}$, then the R_S should have a value below 1.2kΩ according to the above equation.

$$R_S < \frac{1.5}{14\times10^6 \times 5\times10^{-12} \ln\left(2^{12+2}\right)} - 1\text{k}\Omega = 1.2\,\text{k}\Omega$$

ADC Circuit PCB Layout Guidelines

The following PCB layout guidelines are recommended to increase the ADC performance.

- In order to reduce power noise and emissions, the analog power (V_{DDA}) and digital power (V_{DD}) should be separated with a ferrite bead or independently supply the analog and digital power. Also using thicker traces for the MCU power supply and locating decoupling capacitors close to the power supply pins are recommended. These methods will reduce the power inductive impedance, thus effectively reducing noise emissions. The decoupling capacitors should use ceramic capacitors located as close to the power pins of the MCU as possible, and electrolytic capacitors in the vicinity of the PCB power source input.
- A decrease of ADC ground noise can be achieved by partitioning the ground plane into digital and analog domains. These planes should be physically separated by a small gap and connected only at one point with a ferrite bead or metal line that is a few millimeters in size.

- All the ADC channels are located relatively close to each other in the HT32 MCU series. However all the ADC channels are also available for use as digital I/Os. Therefore, it is recommended to avoid assigning digital signal IO function between the analog ADC channels if the electrical design permits this. When this is not possible, try to use extra shielding ground between the digital and analog ADC channel traces. Any grouped ADC channels should also be shielded with an analog ground plane to reduce the amount of crosstalk noise into the ADC block.