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# HT32F61030

## Datasheet

**32-Bit Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ Power Delivery Microcontroller,  
up to 32 KB Flash and 2 KB SRAM with PD3.1, 500 ksps ADC,  
UART, SPI, I<sup>2</sup>C, SCTM, BFTM, RTC and WDT**

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# 1 General Description

The Holtek HT32F61030 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of up to 16 MHz to obtain maximum efficiency. It provides 32 KB of embedded Flash memory for code/data storage and 2 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I<sup>2</sup>C, UART, SPI, SCTM, BFTM, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device integrates USB Power Delivery (PD) PHY communication protocols and are compliant with USB PD 3.1/PPS specification.

The above features ensure that the device is suitable for use in a wide range of PD applications, especially in areas such as power bank, car charger and various products powered by PD protocol.

**arm** CORTEX

## 2 Features

### Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 16 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

### On-Chip Memory

- 32 KB on-chip Flash memory for instruction/data and option byte storage
- 2 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

### Flash Memory Controller – FMC

- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word programming/page erase functions are also provided.

### Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

## Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 16 MHz RC oscillator trimmed to  $\pm 1$  % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK\_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

## Power Management Control Unit – PWRCU

- $V_{DD}$  power supply: 2.5 V ~ 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- $V_{DD}$  and  $V_{CORE}$  power domains
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

## Power Delivery

- Compliant with USB PD 3.1/PPS specification
- Supports Dual Role Port – DRP
- Supports Fast Role Swap – FRS
- Integrated VCONN Switch
- Integrated HVO switch output

Power Delivery has an integrated USB BMC encoding/decoding circuit, it can support Dual Role Port operation, PD 3.1 for allowing up to 240 W power supply and Programmable Power Supply, PPS. The CC1 and CC2 pins is used for Type-C identification and PD communication transmission, providing VCONN power for E-Mark cable. These two pins contain an over voltage protection circuit, which will disconnect the channel to protect the internal circuit when the voltage is too high. There are two HVO output pins used for the external MOS component on/off control.

## External Interrupt/Event Controller – EXTI

- Up to 8 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking



The External Interrupt/Event Controller, EXTI, comprises 8 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

## Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 500 ksps conversion rate
- Up to 8 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include up to 8 external analog signal channels and 2 internal channels which can be measured. There are two conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot and continuous conversion mode.

The internal voltage reference generator (VREF) which can provide a stable ADC reference positive voltage (ADCREFP) and the Band gap of VREF is internally connected to the ADC internal input channel. The precise voltage of the  $V_{REF}$  is individually measured for each part by Holtek during production test.

## I/O Ports – GPIO

- Up to 17 GPIOs
- Port A, B are mapped as 8-line EXTI interrupts
- Almost all I/O pins have configurable output driving current

There are up to 17 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

## Single-Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 8-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 256 to generate the counter clock frequency
- One input Capture function
- Two compare Match Output
- PWM waveform generation with Edge-aligned counting Mode
- Single Pulse Mode Output

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

## Basic Function Timer – BFTM

- 16-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 16-bit up-counting counter designed to measure time intervals and generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

## Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog Timer configuration.

## Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V<sub>CORE</sub> power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

## Inter-integrated Circuit – I<sup>2</sup>C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Supports 7-bit addressing mode and general call addressing
- Supports two 7-bit slave addresses

The I<sup>2</sup>C module is an internal circuit allowing communication with an external I<sup>2</sup>C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I<sup>2</sup>C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I<sup>2</sup>C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception.

## Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to ( $f_{PCLK}/2$ ) MHz for the master mode and ( $f_{PCLK}/3$ ) MHz for the slave mode
- Programmable data frame length up to 8 bits
- FIFO Depth: 4 levels

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence.

## Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to ( $f_{PCLK}/16$ ) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

## Package and Operation Temperature

- 32-pin QFN package
- Operation temperature range: -40 °C to 85 °C

# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

Peripherals		HT32F61030
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		2
Timers	SCTM	3
	BFTM	1
	WDT	1
	RTC	1
Communication	SPI	1
	UART	2
	I <sup>2</sup> C	1
EXTI		8
12-bit ADC		1
Number of channels		Max.8 Channels
Power Delivery		1
GPIO		17 (Max.)
CPU frequency		Up to 16 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		32-pin QFN

Note: The functions listed here, except the Power Delivery, are compatible with the HT32F50030 device. Refer to the HT32F50020/HT32F50030 user manual for detailed functional description.

## Block Diagram

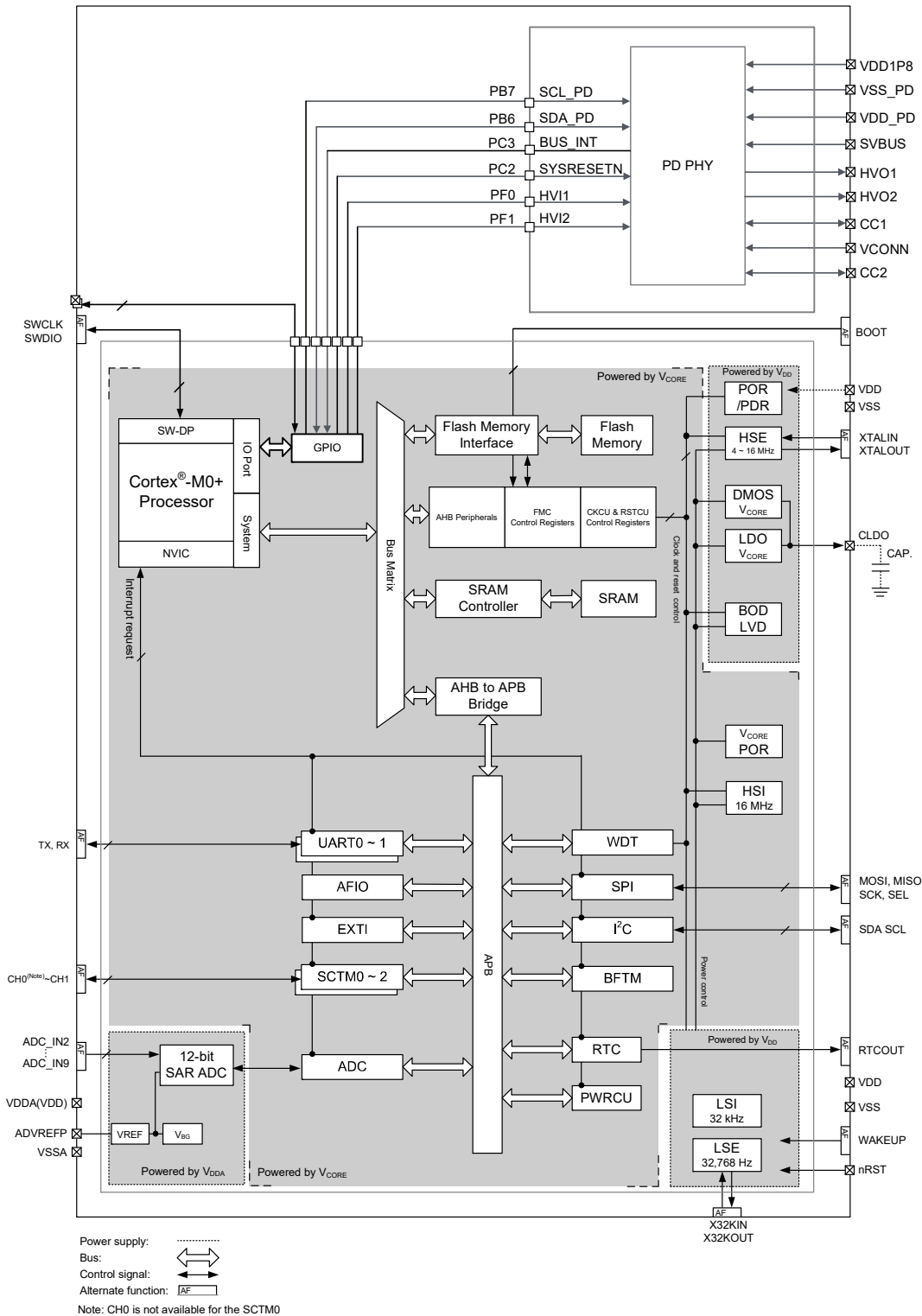


Figure 1. Block Diagram

## Memory Map

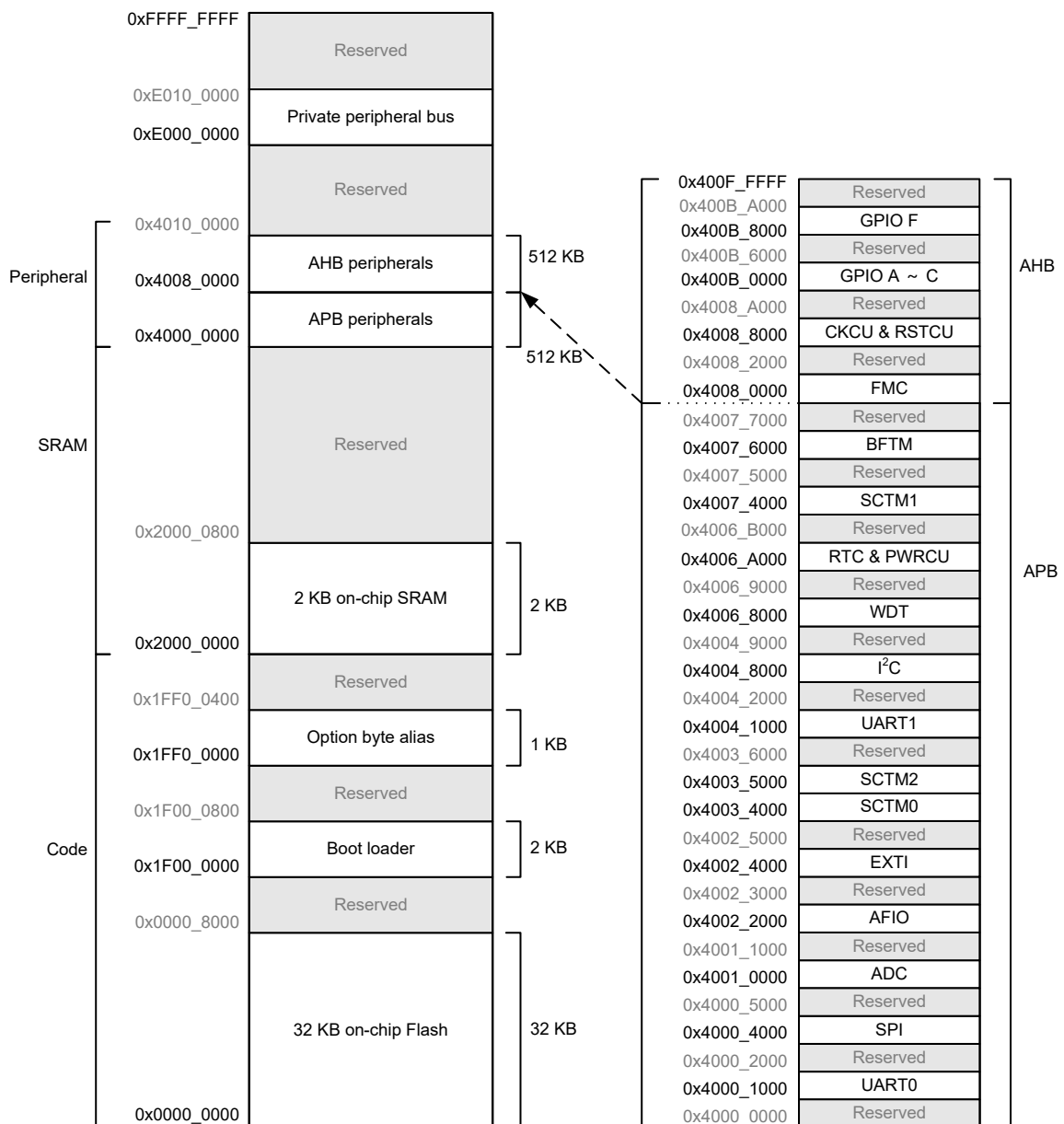


Figure 2. Memory Map

**Table 2. Register Map**

Start Address	End Address	Peripheral	Bus	
0x4000_0000	0x4000_0FFF	Reserved	APB	
0x4000_1000	0x4000_1FFF	UART0		
0x4000_2000	0x4000_3FFF	Reserved		
0x4000_4000	0x4000_4FFF	SPI		
0x4000_5000	0x4000_FFFF	Reserved		
0x4001_0000	0x4001_0FFF	ADC		
0x4001_1000	0x4002_1FFF	Reserved		
0x4002_2000	0x4002_2FFF	AFIO		
0x4002_3000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	EXTI		
0x4002_5000	0x4003_3FFF	Reserved		
0x4003_4000	0x4003_4FFF	SCTM0		
0x4003_5000	0x4003_5FFF	SCTM2		
0x4003_6000	0x4004_0FFF	Reserved		
0x4004_1000	0x4004_1FFF	UART1		
0x4004_2000	0x4004_7FFF	Reserved		
0x4004_8000	0x4004_8FFF	I <sup>2</sup> C		
0x4004_9000	0x4006_7FFF	Reserved		
0x4006_8000	0x4006_8FFF	WDT		
0x4006_9000	0x4006_9FFF	Reserved		
0x4006_A000	0x4006_AFFF	RTC & PWRCU		
0x4006_B000	0x4007_3FFF	Reserved		
0x4007_4000	0x4007_4FFF	SCTM1		
0x4007_5000	0x4007_5FFF	Reserved		
0x4007_6000	0x4007_6FFF	BFTM		
0x4007_7000	0x4007_FFFF	Reserved		
0x4008_0000	0x4008_1FFF	FMC		AHB
0x4008_2000	0x4008_7FFF	Reserved		
0x4008_8000	0x4008_9FFF	CKCU & RSTCU		
0x4008_A000	0x400A_FFFF	Reserved		
0x400B_0000	0x400B_1FFF	GPIO A		
0x400B_2000	0x400B_3FFF	GPIO B		
0x400B_4000	0x400B_5FFF	GPIO C		
0x400B_6000	0x400B_7FFF	Reserved		
0x400B_8000	0x400B_9FFF	GPIO F		
0x400B_A000	0x400F_FFFF	Reserved		

## Clock Structure

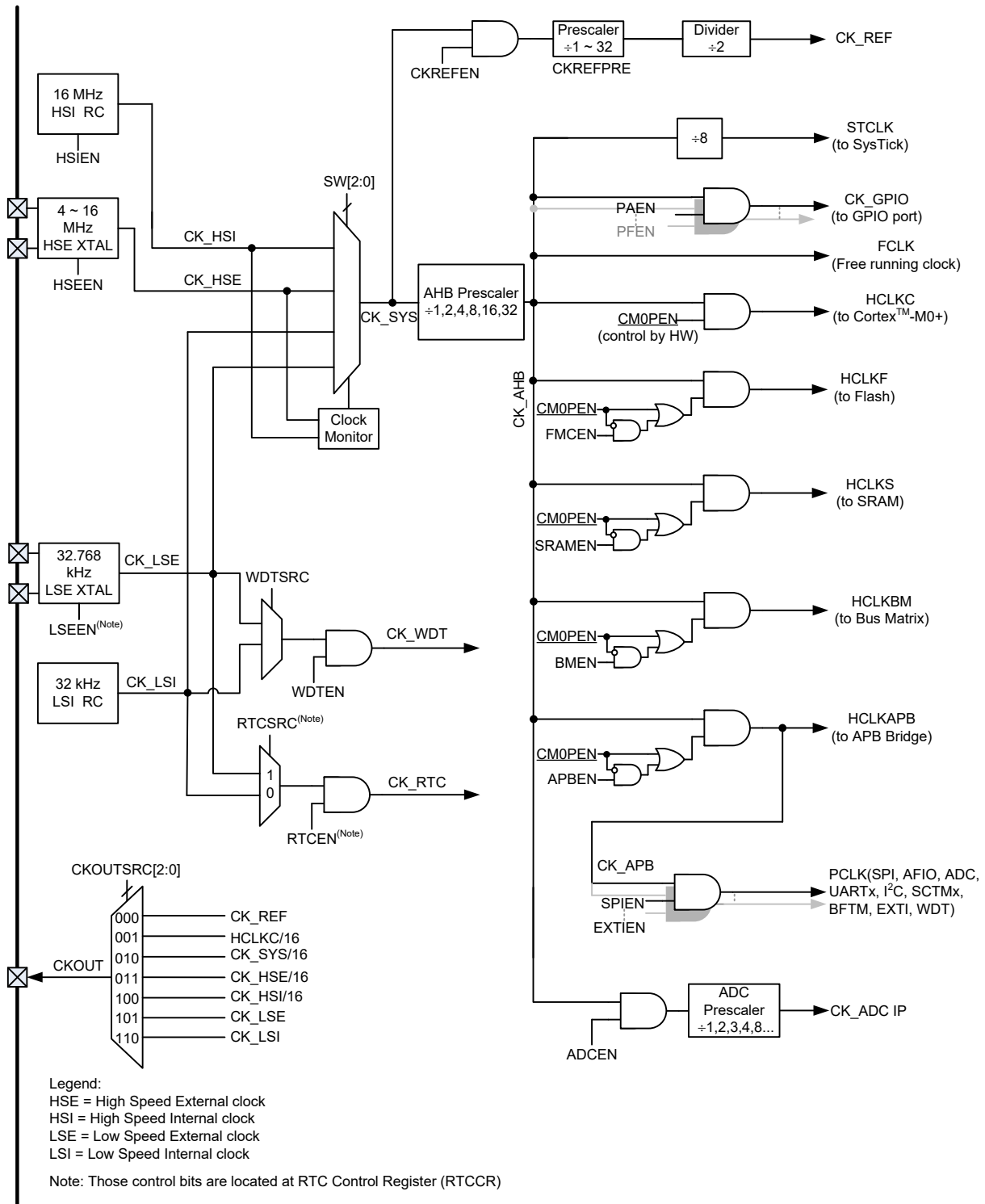


Figure 3. Clock Structure



# 4 PD PHY

Power Delivery, known as PD, is a USB charging standard and technology released by the USB-IF. It uses Type-C interface to implement PD fast charging. With a power output of up to 240 W, it can charge mobile phones, tablet and notebook computers. The high wattage output can even provide power for monitors, televisions, etc., and the Type-C interface can support two-way charging, making it more flexible in use.

The device contains a transceiver control circuit compliant with PD standard. With integrated USB BMC encoding/decoding circuit, it can support Dual Role Port operation, PD 3.1 for allowing up to 240 W power supply and Programmable Power Supply, PPS. The CC1 and CC2 pins is used for Type-C identification and PD communication transmission, providing VCONN power for E-Mark cable. These two pins contain an over voltage protection circuit, which will disconnect the channel to protect the internal circuit when the voltage is too high. There are two HVO output pins used for the external MOS component on/off control. The PD transceiver control circuit contains an independent control register space. The device writes or reads PD register data using the I<sup>2</sup>C interface (master mode) to implement USB Type-C PD communication transmission.

The device has six PD modes. Users can select a PD mode according to their requirements and turn on Type-C detection to start PD communication. When an external PD device is connected, the Type-C identification will automatically be executed. After the identification is completed, an interrupt signal will be generated to inform the device. The device will read data from PD registers using the I<sup>2</sup>C interface and then determine to carry out PD charging or discharging transmission according to the identification result. The PD charge/discharge communication is transmitted and received by MCU writing or reading PD register TX/RX buffer data via the I<sup>2</sup>C interface. The PD protocol communication process is implemented in accordance with PD specification content stipulated by the USB-IF.

## PD PHY Registers Type

Table 3. PD PHY Register Type

Bit Type	Definition
RO	Read only
WC	Write with 1 which in automatically cleared by hardware
RW	Readable and writeable
RWH	Readable and writable which can be overwritten by hardware
RC	Readable interrupt bits, cleared on read

## PD PHY Registers

Overall operation of the PD PHY is controlled using a series of registers.

Table 4. PD PHY Register List

Register Name	Bit							
	7	6	5	4	3	2	1	0
VERSION	INT_RES	—	—	—	—	—	—	—
USB_C_CTL1	DRP_TOG-GL7	DRP_TOG-GL6	DRP_TOG-GL5	CURR_SRC4	CURR_SRC3	MODES2	MODES1	MODES0
USB_C_CTL2	UNSUP_ACC	TRY_SRC	ATT_SRC	ATT_SNK	ERR_REC	DIS_ST	UNATT_SRC	UNATT_SNK

Register Name	Bit							
	7	6	5	4	3	2	1	0
USB_C_CTL3	—	—	VBUS_IGNORE	—	—	RESETPHY	—	DET_DIS
CC1_CONTROL	VBUSOK	—	—	—	PDWN1	TXE1	VCONN1	PU1
CC2_CONTROL	VBUSOK	—	—	—	PDWN2	TXE2	VCONN2	PU2
CC_SEL	—	—	—	—	VCONN_SWAP_OFF	VCONN_SWAP_ON	CC_SEL1	CC_SEL0
USB_C_STATUS1	TYPE_C_DET7	TYPE_C_DET6	CC_ORIENT5	CC_ORIENT4	TYPE_C_RSLT3	TYPE_C_RSLT2	TYPE_C_RSLT1	TYPE_C_RSLT0
USB_C_STATUS2	—	—	VBUS_REQ	PD_NOT_ALLOWED	—	—	OVRTEMP	SHORT
USB_C_STATUS3	TYPE_C_ACTIVE	—	—	—	—	—	—	—
CC1_CMP	—	—	—	DET_3A	DET_1P5A	DET_DEF	DET_RD	DET_RA
CC2_CMP	—	—	—	DET_3A	DET_1P5A	DET_DEF	DET_RD	DET_RA
CC1_STATUS	—	SRC_RX16	SRC_RX15	SRC_RP1	PWR3A_SNK1	PWR1P5A_SNK1	PWRDEF_SNK1	SNK_RP1
CC2_STATUS	—	SRC_RX26	SRC_RX25	SRC_RP2	PWR3A_SNK2	PWR1P5A_SNK2	PWRDEF_SNK2	SNK_RP2
VBUS_MON	VBUS_MON_EN	COMP	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
AFE_TRIM2	—	—	—	—	—	—	TRIM_CCDRV1	TRIM_CCDRV0
AFE_TRIM3	—	TRIM_SLICE2	TRIM_SLICE1	TRIM_SLICE0	—	—	—	—
POWER	VCONN_CTRL_EXT	—	—	—	PWR3	PWR2	PWR1	PWR0
IRQ1	—	—	—	—	I_VBUS_DROP	—	I_OVRTEMP	I_SHORT
IRQ2	I_CC_CHANGE	I_PD_RX	I_PD_HR_RX	I_PD_CR_RX	I_PD_TX_OK	I_PD_TX_FAIL	I_FAST_SWAP	I_TX_DISCARD
IRQ_MSK1	—	—	—	—	M_VBUS_DROP	—	M_OVRTEMP	M_SHORT
IRQ_MSK2	M_CC_CHANGE	M_PD_RX	M_PD_HR_RX	M_PD_CR_RX	M_PD_TX_OK	M_PD_TX_FAIL	M_FAST_SWAP	—
PD_CFG1	ID_INSERT	VBUS_HIGH_VOLT	GUIDE_TRY_SNK	—	RESET_MSG_ID	SOP_TO_RESET2	SOP_TO_RESET1	SOP_TO_RESET0
PD_CFG2	FAST_SWAP_SNK	FAST_SWAP_SRC	CDR_SELECT	SOP_RCV4	SOP_RCV3	SOP_RCV2	SOP_RCV1	SOP_RCV0
PD_CFG3	—	—	P_DATA_ROLE_DP	P_PWR_ROLE_DP	P_DATA_ROLE_PR	P_PWR_ROLE_PR	P_DATA_ROLE_SOP	P_PWR_ROLE_SOP
SHORT_PROTECT	SHORT_RESET	SHORT_TIME6	SHORT_TIME5	SHORT_TIME4	SHORT_TIME3	SHORT_TIME2	SHORT_TIME1	SHORT_TIME0
PD_STATUS	FAST_SWAP	—	RX_RESULT5	RX_RESULT4	RX_RESULT3	TX_RESULT2	TX_RESULT1	TX_RESULT0
RX_STATUS	RX_DATA	RX_OVERRUN	—	—	—	—	—	RX_CLEAR
RX_INFO	RX_BYTES7	RX_BYTES6	RX_BYTES5	RX_BYTES4	RX_BYTES3	RX_SOP2	RX_SOP1	RX_SOP0
TX_COMMAND	TX_CMD7	TX_CMD6	TX_CMD5	—	—	TX_WAIT_RP	TX_START	TXBUF_READY
TX_INFO	—	—	TX_RETRIES5	TX_RETRIES4	TX_RETRIES3	TX_SOP2	TX_SOP1	TX_SOP0

Register Name	Bit							
	7	6	5	4	3	2	1	0
RX_PACKET_DATA61	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA62	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA63	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA64	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA65	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA66	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA67	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA68	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA69	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA70	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA71	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA72	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA73	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA74	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA75	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA76	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA77	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA78	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA79	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA80	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA81	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA82	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA83	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA84	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA85	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA86	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA87	D7	D6	D5	D4	D3	D2	D1	D0

Register Name	Bit							
	7	6	5	4	3	2	1	0
RX_PACKET_DATA88	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA89	D7	D6	D5	D4	D3	D2	D1	D0
RX_PACKET_DATA90	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA91	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA92	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA93	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA94	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA95	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA96	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA97	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA98	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA99	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA100	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA101	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA102	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA103	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA104	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA105	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA106	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA107	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA108	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA109	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA110	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA111	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA112	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA113	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA114	D7	D6	D5	D4	D3	D2	D1	D0

Register Name	Bit							
	7	6	5	4	3	2	1	0
TX_PACKET_DATA115	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA116	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA117	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA118	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA119	D7	D6	D5	D4	D3	D2	D1	D0
TX_PACKET_DATA120	D7	D6	D5	D4	D3	D2	D1	D0
C_OVP	—	—	—	—	ENP2	ENP1	STP2	STP1

The following table indicates the way in which the PD PHY internal registers are affected after a power-on reset occurs.

**Table 5. PD PHY Register Reset List**

Address	Register	Power On Reset
00H	VERSION	0 --- ----
01H	USB_C_CTL1	0000 1000
02H	USB_C_CTL2	0000 0000
03H	USB_C_CTL3	--0- -0-0
04H	CC1_CONTROL	1--- 1000
05H	CC2_CONTROL	1--- 1000
06H	CC_SEL	---- 0000
07H	USB_C_STATUS1	0000 0000
08H	USB_C_STATUS2	--00 --00
09H	USB_C_STATUS3	1 --- ----
0AH	CC1_CMP	---0 0000
0BH	CC2_CMP	---0 0000
0CH	CC1_STATUS	-000 0000
0DH	CC2_STATUS	-000 0000
0FH	VBUS_MON	0000 0000
11H	AFE_TRIM2	---- --10
12H	AFE_TRIM3	-000 ----
14H	POWER	0--- 1111
16H	IRQ1	---- 0-00
17H	IRQ2	1000 0000
18H	IRQ_MSK1	---- 0-00
19H	IRQ_MSK2	0000 000-
1AH	PD_CFG1	000- 0000
1BH	PD_CFG2	0000 0000
1CH	PD_CFG3	--00 0000
1DH	SHORT_PROTECT	0010 1001
1EH	PD_STATUS	0-00 0000
1FH	RX_STATUS	00-- ---0
20H	RX_INFO	0000 0000

Address	Register	Power On Reset
21H	TX_COMMAND	000- -001
22H	TX_INFO	--01 1000
3DH	RX_PACKET_DATA61	0000 0000
3EH	RX_PACKET_DATA62	0000 0000
3FH	RX_PACKET_DATA63	0000 0000
40H	RX_PACKET_DATA64	0000 0000
41H	RX_PACKET_DATA65	0000 0000
42H	RX_PACKET_DATA66	0000 0000
43H	RX_PACKET_DATA67	0000 0000
44H	RX_PACKET_DATA68	0000 0000
45H	RX_PACKET_DATA69	0000 0000
46H	RX_PACKET_DATA70	0000 0000
47H	RX_PACKET_DATA71	0000 0000
48H	RX_PACKET_DATA72	0000 0000
49H	RX_PACKET_DATA73	0000 0000
4AH	RX_PACKET_DATA74	0000 0000
4BH	RX_PACKET_DATA75	0000 0000
4CH	RX_PACKET_DATA76	0000 0000
4DH	RX_PACKET_DATA77	0000 0000
4EH	RX_PACKET_DATA78	0000 0000
4FH	RX_PACKET_DATA79	0000 0000
50H	RX_PACKET_DATA80	0000 0000
51H	RX_PACKET_DATA81	0000 0000
52H	RX_PACKET_DATA82	0000 0000
53H	RX_PACKET_DATA83	0000 0000
54H	RX_PACKET_DATA84	0000 0000
55H	RX_PACKET_DATA85	0000 0000
56H	RX_PACKET_DATA86	0000 0000
57H	RX_PACKET_DATA87	0000 0000
58H	RX_PACKET_DATA88	0000 0000
59H	RX_PACKET_DATA89	0000 0000
5AH	RX_PACKET_DATA90	0000 0000
5BH	TX_PACKET_DATA91	0000 0000
5CH	TX_PACKET_DATA92	0000 0000
5DH	TX_PACKET_DATA93	0000 0000
5EH	TX_PACKET_DATA94	0000 0000
5FH	TX_PACKET_DATA95	0000 0000
60H	TX_PACKET_DATA96	0000 0000
61H	TX_PACKET_DATA97	0000 0000
62H	TX_PACKET_DATA98	0000 0000
63H	TX_PACKET_DATA99	0000 0000
64H	TX_PACKET_DATA100	0000 0000
65H	TX_PACKET_DATA101	0000 0000
66H	TX_PACKET_DATA102	0000 0000
67H	TX_PACKET_DATA103	0000 0000
68H	TX_PACKET_DATA104	0000 0000

Address	Register	Power On Reset
69H	TX_PACKET_DATA105	0000 0000
6AH	TX_PACKET_DATA106	0000 0000
6BH	TX_PACKET_DATA107	0000 0000
6CH	TX_PACKET_DATA108	0000 0000
6DH	TX_PACKET_DATA109	0000 0000
6EH	TX_PACKET_DATA110	0000 0000
6FH	TX_PACKET_DATA111	0000 0000
70H	TX_PACKET_DATA112	0000 0000
71H	TX_PACKET_DATA113	0000 0000
72H	TX_PACKET_DATA114	0000 0000
73H	TX_PACKET_DATA115	0000 0000
74H	TX_PACKET_DATA116	0000 0000
75H	TX_PACKET_DATA117	0000 0000
76H	TX_PACKET_DATA118	0000 0000
77H	TX_PACKET_DATA119	0000 0000
78H	TX_PACKET_DATA120	0000 0000
7DH	C_OVP	---- 0000

• **VERSION Register**

Bit	7	6	5	4	3	2	1	0
Name	INT_RES	—	—	—	—	—	—	—
R/W	R/W	RO	RO	RO	RO	RO	RO	RO
POR	0	0	0	0	0	1	1	1

- Bit 7      **INT\_RES**: Interrupts Reset control  
             0: Reset interrupts by reading  
             1: Reset interrupts by writing “1” to the bits to be cleared
- Bit 6~0      Unimplemented, read as “0”

• **USB\_C\_CTL1 Register**

Bit	7	6	5	4	3	2	1	0
Name	DRP_TOGGL7	DRP_TOGGL6	DRP_TOGGL5	CURR_SRC4	CURR_SRC3	MODES2	MODES1	MODES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	1	0	0	0

- Bit 7~5      **DRP\_TOGGL7~DRP\_TOGGL5**: Type-C State Machine configuration  
             000: 50 % in Unattached.SNK State and 50 % in Unattached.SRC  
             001: 40 % in Unattached.SNK State and 60 % in Unattached.SRC  
             010: 30 % in Unattached.SNK State and 70 % in Unattached.SRC  
             011: Reserved  
             100: Reserved  
             101: 60 % in Unattached.SNK State and 40 % in Unattached.SRC  
             110: 70 % in Unattached.SNK State and 30 % in Unattached.SRC  
             111: Pseudo randomly change the ratio between Unattached.SNK and Unattached.SRC between 34 % and 66 %

- Bit 4~3     **CURR\_SRC4~CURR\_SRC3**: R<sub>p</sub> pull-up current selection  
           00: No current  
           01: 80 μA – Default current capability  
           10: 180 μA – 1.5 A current capability  
           11: 330 μA – 3 A current capability
- Bit 2~0     **MODES2~MODE0**: PD mode selection  
           000: SNK (start in sink mode. No Accessory support.)  
           001: SNK + Accessory Support  
           010: SRC (start in source mode. No Accessory support.)  
           011: SRC + Accessory Support  
           100: DRP (dual role port – will toggle (refer to the DRP\_TOGGL[7:5] bits)  
           101: DRP + Accessory Support  
           110: Reserved  
           111: Reserved

Note: This bit field selects which State Machine is used. The ATT\_SRC and ATT\_SNK bits can be used to switch state machines between source and sink during PR-swap (refer to the USB\_C\_CTL2 register).

• **USB\_C\_CTL2 Register**

Bit	7	6	5	4	3	2	1	0
Name	UNSUP_ACC	TRY_SRC	ATT_SRC	ATT_SNK	ERR_REC	DIS_ST	UNATT_SRC	UNATT_SNK
R/W	WC	R/W	WC	WC	WC	WC	WC	WC
POR	0	0	0	0	0	0	0	0

- Bit 7     **UNSUP\_ACC**: Unsupported Accessory control  
           0: No effect  
           1: Unsupported Accessory – use if software does not know how to support this accessory  
           When this bit is set high, go to the Unsupported Accessory state if the software does not support this powered accessory.
- Bit 6     **TRY\_SRC**: TRY.SRC mode control  
           0: No effect  
           1: TRY.SRC mode enabled
- Bit 5     **ATT\_SRC**: Attached.SRC control  
           0: No effect  
           1: Set Type-C circuit in Attached.SRC State  
           When this bit is set high, go to Attached.SRC state, done with a Power Role Swap and valid only from Attached.SNK state.
- Bit 4     **ATT\_SNK**: Attached.SNK control  
           0: No effect  
           1: Set Type-C circuit in Attached.SNK State  
           When this bit is set high, go to Attached.SNK state, done with a Power Role Swap and valid only from Attached.SRC state.
- Bit 3     **ERR\_REC**: Type-C circuit ErrorRecovery State control  
           0: No effect  
           1: Set Type-C circuit in ErrorRecovery State  
           When this bit is set high, go to ErrorRecovery state, valid from any state.
- Bit 2     **DIS\_ST**: Type-C circuit Disabled State control  
           0: No effect  
           1: Set Type-C circuit in Disabled State  
           When this bit is set high, go to Disabled state, valid from any state.



- Bit 1      **UNATT\_SRC**: Type-C circuit Unattached.SRC State control  
0: No effect  
1: Set Type-C circuit in Unattached.SRC State – provided the FSM is in an appropriate state
- Bit 0      **UNATT\_SNK**: Type-C circuit Unattached.SNK State control  
0: No effect  
1: Set Type-C circuit in Unattached.SNK State – provided the FSM is in an appropriate state

• **USB\_C\_CTL3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	VBUS_IGNORE	—	—	RESETPHY	—	DET_DIS
R/W	—	—	R/W	—	—	WC	—	R/W
POR	—	—	0	—	—	0	—	0

- Bit 7~6      Unimplemented, read as “0”
- Bit 5      **VBUS\_IGNORE**: VBUS ignore selection  
0: Use VBUS for state change  
1: Ignore VBUS during PR-swap
- Bit 4~3      Unimplemented, read as “0”
- Bit 2      **RESETPHY**: PD PHY logic reset control  
0: Normal operation  
1: Force reset of PD logic – Does not reset registers
- Bit 1      Unimplemented, read as “0”
- Bit 0      **DET\_DIS**: Type-C detection control  
0: Type-C detection enabled  
1: Type-C detection disabled – Control only by software, ignore FSM

• **CC1\_CONTROL Register**

Bit	7	6	5	4	3	2	1	0
Name	VBUSOK	—	—	—	PDWN1	TXE1	VCONN1	PU1
R/W	RO	—	—	—	RWH	RWH	RWH	RWH
POR	1	—	—	—	1	0	0	0

- Bit 7      **VBUSOK**: VBUS active status  
0: VBUS is not active  
1: VBUS is active
- Bit 6~4      Unimplemented, read as “0”
- Bit 3      **PDWN1**: 5.1 kΩ pull down resistor to CC1 control  
0: Disable  
1: Enable
- Bit 2      **TXE1**: CC1 PD driver control  
0: Disable  
1: Enable
- Bit 1      **VCONN1**: VCONN power to CC1 control  
0: Disable  
1: Enable
- Bit 0      **PU1**: Pull up current to CC1 control  
0: Disable  
1: Enable

• **CC2\_CONTROL Register**

Bit	7	6	5	4	3	2	1	0
Name	VBUSOK	—	—	—	PDWN2	TXE2	VCONN2	PU2
R/W	RO	—	—	—	RWH	RWH	RWH	RWH
POR	1	—	—	—	1	0	0	0

- Bit 7        **VBUSOK**: VBUS active status  
0: VBUS is not active  
1: VBUS is active
- Bit 6~4     Unimplemented, read as “0”
- Bit 3        **PDWN2**: 5.1 kΩ pull down resistor to CC2 control  
0: Disable  
1: Enable
- Bit 2        **TXE2**: CC2 PD driver control  
0: Disable  
1: Enable
- Bit 1        **VCONN2**: VCONN power to CC2 control  
0: Disable  
1: Enable
- Bit 0        **PU2**: Pull up current to CC2 control  
0: Disable  
1: Enable

• **CC\_SEL Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	VCONN_SWAP_OFF	VCONN_SWAP_ON	CC_SEL1	CC_SEL0
R/W	—	—	—	—	WC	WC	RWH	RWH
POR	—	—	—	—	0	0	0	0

- Bit 7~4     Unimplemented, read as “0”
- Bit 3        **VCONN\_SWAP\_OFF**: VCONN via Type-C FSM control  
0: Reserved  
1: Turn off
- Bit 2        **VCONN\_SWAP\_ON**: VCONN via Type-C FSM control  
0: Reserved  
1: Turn on
- Bit 1~0     **CC\_SEL1~CC\_SEL0**: CC2 PD driver control  
00: Reserved  
01: CC1 select  
10: CC2 select  
11: Reserved

• **USB\_C\_STATUS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	TYPE_C_DET7	TYPE_C_DET6	CC_ORIENT5	CC_ORIENT4	TYPE_C_RSLT3	TYPE_C_RSLT2	TYPE_C_RSLT1	TYPE_C_RSLT0
R/W	RO	RO	RO	RO	RO	RO	RO	RO
POR	0	0	0	0	0	0	0	0

- Bit 7~6     **TYPE\_C\_DET7~TYPE\_C\_DET6:** Type-C detection status  
 00: Type-C detection has not started  
 01: Type-C detection is ongoing  
 10: Type-C detection is completed (Type-C result may be read)  
 11: Reserved
- Bit 5~4     **CC\_ORIENT5~CC\_ORIENT4:** CC1/CC2 connection status  
 00: No or unresolved connection is detected  
 01: Position 1 (Normal Orientation – CC1)  
 10: Position 2 (Normal Orientation – CC2)  
 11: A fault has occurred during detection
- Bit 3~0     **TYPE\_C\_RSLT3~TYPE\_C\_RSLT0:** Type-C detection result status  
 0000: Nothing is attached  
 0001: SRC with Default current capability is attached  
 0010: SRC with 1.5 A current capability is attached  
 0011: SRC with 3 A current capability is attached  
 0100: SNK is attached  
 0101: Debug Accessory is attached  
 0110: Audio Accessory is attached  
 0111: Powered Accessory is attached  
 1000~1110: Reserved  
 1111: Undetermined

• **USB\_C\_STATUS2 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	VBUS_REQ	PD_NOT_ALLOWED	—	—	OVRTEMP	SHORT
R/W	—	—	RO	RO	—	—	RO	RO
POR	—	—	0	0	—	—	0	0

- Bit 7~6     Unimplemented, read as “0”
- Bit 5     **VBUS\_REQ:** Indicates the state the VBUS switch should be on  
 0: VBUS is not required  
 1: VBUS is now required
- Bit 4     **PD\_NOT\_ALLOWED:** PD allowed status  
 0: PD is allowed  
 1: PD is not allowed
- Bit 3~2     Unimplemented, read as “0”
- Bit 1     **OVRTEMP:** Over temperature status  
 0: Not over temperature  
 1: Over temperature

Bit 0      **SHORT**: Reflect short logic input  
This indicates that the VCONN output voltage switch is on and there is an unsafe voltage across it. This signal will typically glitch when VCONN is turned on, and remain high during an overcurrent situation. A sustained short signal will cause an I\_SHORT interrupt. Hence this bit is normally used only for debug.

• **USB\_C\_STATUS3 Register**

Bit	7	6	5	4	3	2	1	0
Name	TYPEC_ACTIVE	—	—	—	—	—	—	—
R/W	RO	—	—	—	—	—	—	—
POR	1	—	—	—	—	—	—	—

Bit 7      **TYPEC\_ACTIVE**: FSM active status  
0: FSM is not active  
1: FSM is active

Bit 6~0      Unimplemented, read as “0”

• **CC1\_CMP Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	DET_3A	DET_1P5A	DET_DEF	DET_RD	DET_RA
R/W	—	—	—	RO	RO	RO	RO	RO
POR	—	—	—	0	0	0	0	0

Bit 7~5      Unimplemented, read as “0”

Bit 4      **DET\_3A**: CC1 3 A detection status  
0: 3 A is not detected  
1: 3 A is detected

Bit 3      **DET\_1P5A**: CC1 1.5 A detection status  
0: 1.5 A is not detected  
1: 1.5 A is detected

Bit 2      **DET\_DEF**: CC1 default current detection status  
0: Default current is not detected  
1: Default current is detected

Bit 1      **DET\_RD**: CC1 R<sub>D</sub> detection status  
0: R<sub>D</sub> is not detected  
1: R<sub>D</sub> is detected

Bit 0      **DET\_RA**: CC1 R<sub>A</sub> detection status  
0: R<sub>A</sub> is not detected  
1: R<sub>A</sub> is detected

• **CC2\_CMP Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	DET_3A	DET_1P5A	DET_DEF	DET_RD	DET_RA
R/W	—	—	—	RO	RO	RO	RO	RO
POR	—	—	—	0	0	0	0	0

Bit 7~5      Unimplemented, read as “0”

Bit 4      **DET\_3A**: CC2 3 A detection status  
0: 3 A is not detected  
1: 3 A is detected

- Bit 3     **DET\_1P5A**: CC2 1.5 A detection status  
          0: 1.5 A is not detected  
          1: 1.5 A is detected
- Bit 2     **DET\_DEF**: CC2 default current detection status  
          0: Default current is not detected  
          1: Default current is detected
- Bit 1     **DET\_RD**: CC2 R<sub>D</sub> detection status  
          0: R<sub>D</sub> is not detected  
          1: R<sub>D</sub> is detected
- Bit 0     **DET\_RA**: CC2 R<sub>A</sub> detection status  
          0: R<sub>A</sub> is not detected  
          1: R<sub>A</sub> is detected

• **CC1\_STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	—	SRC_ RX16	SRC_ RX15	SRC_ RP1	PWR3A_ SNK1	PWR1P5A_ SNK1	PWRDEF_ SNK1	SNK_ RP1
R/W	—	RO	RO	RO	RO	RO	RO	RO
POR	—	0	0	0	0	0	0	0

- Bit 7     Unimplemented, read as “0”
- Bit 6~5   **SRC\_RX16~SRC\_RX15**: CC1 SRC detection status  
          00: Nothing is detected after t<sub>CCDebounce</sub> (SRC.open)  
          01: R<sub>D</sub> is detected after t<sub>CCDebounce</sub> (SRC.R<sub>D</sub>)  
          10: R<sub>A</sub> is detected after t<sub>CCDebounce</sub> (SRC.R<sub>A</sub>)  
          11: Reserved
- Bit 4     **SRC\_RP1**: CC1 SRC detection status  
          0: Nothing is detected (CC1 above maximum V<sub>RD</sub>)  
          1: R<sub>D</sub> or R<sub>A</sub> pull-down is detected (CC1 below maximum V<sub>RD</sub>)
- Bit 3     **PWR3A\_SNK1**: CC1 SNK 3 A detection status  
          0: Nothing is detected  
          1: SRC with 3 A current capability is detected
- Bit 2     **PWR1P5A\_SNK1**: CC1 SNK 1.5 A detection status  
          0: Nothing is detected  
          1: SRC with 1.5 A current capability is detected
- Bit 1     **PWRDEF\_SNK1**: CC1 SNK default current detection status  
          0: Nothing is detected  
          1: SRC with default current capability is detected
- Bit 0     **SNK\_RP1**: CC1 SNK R<sub>P</sub> detection status  
          0: Nothing is detected (CC1 below maximum V<sub>RA</sub>) (SNK.open)  
          1: R<sub>P</sub> pull-up is detected (CC1 above minimum V<sub>RD</sub>) (SNK.R<sub>P</sub>)

• **CC2\_STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	—	SRC_RX26	SRC_RX25	SRC_RP2	PWR3A_SNK2	PWR3A_SNK2	PWRDEF_SNK2	SNK_RP2
R/W	—	RO	RO	RO	RO	RO	RO	RO
POR	—	0	0	0	0	0	0	0

- Bit 7 Unimplemented, read as “0”
- Bit 6~5 **SRC\_RX26~SRC\_RX25**: CC2 SRC detection status  
 00: Nothing is detected after  $t_{CCDebounce}$  (SRC.open)  
 01:  $R_D$  is detected after  $t_{CCDebounce}$  (SRC. $R_D$ )  
 10:  $R_A$  is detected after  $t_{CCDebounce}$  (SRC. $R_A$ )  
 11: Reserved
- Bit 4 **SRC\_RP2**: CC2 SRC detection status  
 0: Nothing is detected (CC2 above maximum  $V_{RD}$ )  
 1:  $R_D$  or  $R_A$  pull-down is detected (CC2 below maximum  $V_{RD}$ )
- Bit 3 **PWR3A\_SNK2**: CC2 SNK 3 A detection status  
 0: Nothing is detected  
 1: SRC with 3 A current capability is detected
- Bit 2 **PWR1P5A\_SNK2**: CC2 SNK 1.5 A detection status  
 0: Nothing is detected  
 1: SRC with 1.5 A current capability is detected
- Bit 1 **PWRDEF\_SNK2**: CC2 SNK default current detection status  
 0: Nothing is detected  
 1: SRC with default current capability is detected
- Bit 0 **SNK\_RP2**: CC2 SNK  $R_p$  detection status  
 0: Nothing is detected (CC2 below maximum  $V_{RA}$ ) (SNK.open)  
 1:  $R_p$  pull-up is detected (CC2 above minimum  $V_{RD}$ ) (SNK. $R_p$ )

• **VBUS\_MON Register**

Bit	7	6	5	4	3	2	1	0
Name	VBUS_MON_EN	COMP	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
R/W	R/W	RO	RWH	RWH	RWH	RWH	RWH	RWH
POR	0	0	0	0	0	0	0	0

- Bit 7 **VBUS\_MON\_EN**: VBUS monitor comparator control  
 0: Disable  
 1: Enable
- Bit 6 **COMP**: VBUS higher than DAC set threshold  
 0: VBUS is not higher  
 1: VBUS is higher
- Bit 5~0 **DAC5~DAC0**: Scaled VBUS threshold value  
 For 48 V EPR configuration, a 6-bit DAC is used to detect voltage drop. With recommended external divider, the following method is used to set the VBUS voltage when voltage drop detection is required:  
 $DAC = 1.5 \times (VBUS - 6)$

● **AFE\_TRIM2 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	TRIM_CCDRV1	TRIM_CCDRV0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	1	0

Bit 7~2 Unimplemented, read as “0”

Bit 1~0 **TRIM\_CCDRV1~TRIM\_CCDRV0**: CC driver rise/fall trim  
00: Slowest  
01~10: Mid-point  
11: Fastest

● **AFE\_TRIM3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	TRIM_SLICE2	TRIM_SLICE1	TRIM_SLICE0	—	—	—	—
R/W	—	R/W	R/W	R/W	—	—	—	—
POR	—	0	0	0	—	—	—	—

Bit 7 Unimplemented, read as “0”

Bit 6~4 **TRIM\_SLICE2~TRIM\_SLICE0**: Trim for the slicer when CDR\_SELECT=1  
The valid values are 3’h4 : 3’h0, with 3’h2 being the mid position of the trim. It is likely that after characterization these bits can be fixed, and always set to the same value on boot. Use a default value of 3’h7.

Bit 3~0 Unimplemented, read as “0”

● **POWER Register**

Bit	7	6	5	4	3	2	1	0
Name	VCONN_CTRL_EXT	—	—	—	PWR3	PWR2	PWR1	PWR0
R/W	R/W	—	—	—	R/W	R/W	R/W	R/W
POR	0	—	—	—	1	1	1	1

Bit 7 **VCONN\_CTRL\_EXT**: External VCONN generator enable control  
0: Use internal VCONN generator  
1: Use external VCONN generator

Bit 6~4 Unimplemented, read as “0”

Bit 3~0 **PWR3~PWR0**: Power enable control  
0000: All Disable  
0001: AFE Power Enable  
0010: Wake Power Enable  
0100: Bandgap and LDO Power Enable  
1000: Oscillator Enable  
1101: AFE Power, Bandgap and LDO Power, Oscillator Enable  
1111: AFE Power, Wake Power, Bandgap and LDO Power, Oscillator Enable  
Others: Reserved

• **IRQ1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	I_VBUS_DROP	—	I_OVRTEMP	I_SHORT
R/W	—	—	—	—	RC	—	RC	RC
POR	—	—	—	—	0	—	0	0

- Bit 7~4      Unimplemented, read as “0”
- Bit 3      **I\_VBUS\_DROP**: Indicates VBUS has dropped below threshold set by DAC[5:0]  
0: VBUS is not dropped below threshold  
1: VBUS is dropped below threshold
- Bit 2      Unimplemented, read as “0”
- Bit 1      **I\_OVRTEMP**: OTP interrupt  
0: OTP is not interrupt  
1: OTP is interrupt
- Bit 0      **I\_SHORT**: Short interrupt  
0: Short is not interrupt  
1: Short is interrupt

• **IRQ2 Register**

Bit	7	6	5	4	3	2	1	0
Name	I_CC_CHANGE	I_PD_RX	I_PD_HR_RX	I_PD_CR_RX	I_PD_TX_OK	I_PD_TX_FAIL	I_FAST_SWAP	I_TX_DISCARD
R/W	RC	RC	RC	RC	RC	RC	RC	RC
POR	1	0	0	0	0	0	0	0

- Bit 7      **I\_CC\_CHANGE**: Type-C status changed  
0: Type-C status is not changed  
1: Type-C status is changed
- Bit 6      **I\_PD\_RX**: PD-message received  
0: PD-message is not received  
1: PD-message is received
- Bit 5      **I\_PD\_HR\_RX**: PD-HardReset received  
0: PD-HardReset is not received  
1: PD-HardReset is received
- Bit 4      **I\_PD\_CR\_RX**: PD-CableReset received  
0: PD-CableReset is not received  
1: PD-CableReset is received
- Bit 3      **I\_PD\_TX\_OK**: PD-Transmit success  
0: PD-Transmit is not success  
1: PD-Transmit is success
- Bit 2      **I\_PD\_TX\_FAIL**: PD-Transmit failure  
0: PD-Transmit is not failure  
1: PD-Transmit is failure
- Bit 1      **I\_FAST\_SWAP**: Fast Role Swap occurred  
0: Fast Role Swap is not occurred  
1: Fast Role Swap is occurred
- Bit 0      **I\_TX\_DISCARD**: PD transmit discarded due to incoming message  
0: PD transmit was not discarded  
1: PD transmit was discarded  
Refer to the TX\_RESULT[2:0] bits in the PD\_STATUS register.



• **IRQ\_MSK1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	M_VBUS_DROP	—	M_OVRTEMP	M_SHORT
R/W	—	—	—	—	R/W	—	R/W	R/W
POR	—	—	—	—	0	—	0	0

- Bit 7~4 Unimplemented, read as “0”
- Bit 3 **M\_VBUS\_DROP**: VBUS\_DROP interrupt control  
0: Disable  
1: Enable
- Bit 2 Unimplemented, read as “0”
- Bit 1 **M\_OVRTEMP**: OTP interrupt control  
0: Disable  
1: Enable
- Bit 0 **M\_SHORT**: Short interrupt control  
0: Disable  
1: Enable

• **IRQ\_MSK2 Register**

Bit	7	6	5	4	3	2	1	0
Name	M_CC_CHANGE	M_PD_RX	M_PD_HR_RX	M_PD_CR_RX	M_PD_TX_OK	M_PD_TX_FAIL	M_FAST_SWAP	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	0	0	0	0	0	0	0	—

- Bit 7 **M\_CC\_CHANGE**: Type-C status changed interrupt control  
0: Disable  
1: Enable
- Bit 6 **M\_PD\_RX**: PD-message received interrupt control  
0: Disable  
1: Enable
- Bit 5 **M\_PD\_CR\_RX**: PD-HardReset received interrupt control  
0: Disable  
1: Enable
- Bit 4 **M\_PD\_TX\_OK**: PD-CableReset received interrupt control  
0: Disable  
1: Enable
- Bit 3 **M\_VBUS\_DROP**: PD-Transmit success interrupt control  
0: Disable  
1: Enable
- Bit 2 **M\_PD\_TX\_FAIL**: PD-Transmit failure interrupt control  
0: Disable  
1: Enable
- Bit 1 **M\_FAST\_SWAP**: Fast Role Swap interrupt control  
0: Disable  
1: Enable
- Bit 0 Unimplemented, read as “0”

• **PD\_CFG1 Register**

Bit	7	6	5	4	3	2	1	0
Name	ID_INSERT	VBUS_HIGH_VOLT	GUIDE_TRY_SNK	—	RESET_MSG_ID	SOP_TO_RESET2	SOP_TO_RESET1	SOP_TO_RESET0
R/W	R/W	R/W	R/W	—	WC	R/W	R/W	R/W
POR	0	0	0	—	0	0	0	0

- Bit 7      **ID\_INSERT**: PD-FSM status control  
 0: PD-FSM will not change outgoing message – In this case software is responsible for providing the ID bits in the header  
 1: PD-FSM will keep track of Transmitted IDs for all SOP\* and insert the correct value into the header at bit 11 ~ bit 9, no other bits are touched
- Bit 6      **VBUS\_HIGH\_VOLT**: PD-FSM BIST Mode 2 control  
 0: PD-FSM will respond to request for BIST Mode 2 for compliance  
 1: PD-FSM will not respond to request for BIST Mode 2 for compliance  
 Note: The software must keep this bit updated according to VBUS voltage. Set to 1 if VBUS is above vSafe5V. This is required by the specification. Note that the original purpose of this was to prevent malicious use of BIST to force a port to high voltage which continues even after disconnect. However, the specification now limits the BIST length to 60 ms.
- Bit 5      **GUIDE\_TRY\_SNK**: Use the TRY\_SINK modified Type-C FSM  
 0: Not use  
 1: Use
- Bit 4      Unimplemented, read as “0”
- Bit 3      **RESET\_MSG\_ID**: Write 1 to clear the MessageID for SOP\_TO\_RESET type messages control  
 0: Reserved  
 1: Clear the MessageID
- Bit 2~0    **SOP\_TO\_RESET2~SOP\_TO\_RESET0**: Which SOP to reset MessageID for  
 Typically used to reset ID during a swap operation  
 001: SOP  
 010: SOP’  
 010: SOP’’  
 100: Debug\_SOP  
 101: Debug\_SOP’’  
 110~111: Reserved

• **PD\_CFG2 Register**

Bit	7	6	5	4	3	2	1	0
Name	FAST_SWAP_SNK	FAST_SWAP_SRC	CDR_SELECT	SOP_RCV4	SOP_RCV3	SOP_RCV2	SOP_RCV1	SOP_RCV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7      **FAST\_SWAP\_SNK**: Fast Role Swap sink function enable control  
 0: Disable  
 1: Enable
- Bit 6      **FAST\_SWAP\_SRC**: Fast Role Swap source function enable control  
 0: Disable  
 1: Enable

Bit 5 **CDR\_SELECT**: Select between versions of the CC CDR  
0: 3-level slicer  
1: AC coupled

Note that this bit also controls rxMode signals to the AFE.

Bit 4~0 **SOP\_RCV4~SOP\_RCV0**: Select which SOP to receive  
0000: No SOP is received  
xxxx1: SOP is received  
xxx1x: SOP' is received  
xx1xx: SOP'' is received  
x1xxx: SOP\_debug' is received  
1xxxx: SOP\_debug'' is received

Note that multiple SOP types can be received at the same time.

• **PD\_CFG3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	P_DATA_ROLE_DP	P_PWR_ROLE_DP	P_DATA_ROLE_PR	P_PWR_ROLE_PR	P_DATA_ROLE_SOP	P_PWR_ROLE_SOP
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as “0”

Bit 5 **P\_DATA\_ROLE\_DP**: SOP''. Current Port Data Role. Transmit header bit 5  
0: Bit is cleared to 0  
1: Bit is set to 1

Cable communication to the remote end of the cable (future use).

Bit 4 **P\_PWR\_ROLE\_DP**: SOP''. Current Port Power Role. Transmit header bit 8  
Cable communication to the remote end of the cable (future use).  
0: Bit is cleared to 0  
1: Bit is set to 1

Bit 3 **P\_DATA\_ROLE\_PR**: SOP'. Current Port Data Role. Transmit header bit 5  
0: Bit is cleared to 0  
1: Bit is set to 1

Cable communication to the near end of the cable.

Bit 2 **P\_PWR\_ROLE\_PR**: SOP'. Current Port Power Role. Transmit header bit 8  
0: Bit is cleared to 0  
1: Bit is set to 1

Cable communication to the near end of the cable.

Bit 1 **P\_DATA\_ROLE\_SOP**: SOP. Current Port Data Role. Transmit header bit 5  
0: Bit is cleared to 0  
1: Bit is set to 1

Bit 0 **P\_PWR\_ROLE\_SOP**: SOP. Current Port Power Role. Transmit header bit 8  
0: Bit is cleared to 0  
1: Bit is set to 1

• **SHORT\_PROTECT Register**

Bit	7	6	5	4	3	2	1	0
Name	SHORT_RESET	SHORT_TIME6	SHORT_TIME5	SHORT_TIME4	SHORT_TIME3	SHORT_TIME2	SHORT_TIME1	SHORT_TIME0
R/W	WC	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	1	0	0	1

Bit 7~6 **SHORT\_RESET**: Short reset control

0: Reserved

1: Reset

Note: 1. Write 1 to reset VCONN power after maximum short time has been reached.

2. To prevent over-temperature, protect should not be reset more than once per second.

Bit 6~0 **SHORT\_TIME6~SHORT\_TIME0**: Maximum short time before VCONN is shut off

– One LSB is 0.488 ms

• **PD\_STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	FAST_SWAP	—	RX_RESULT5	RX_RESULT4	RX_RESULT3	TX_RESULT2	TX_RESULT1	TX_RESULT0
R/W	RO	—	RO	RO	RO	RO	RO	RO
POR	0	—	0	0	0	0	0	0

Bit 7 **FAST\_SWAP**: Indicates Fast Role Swap has happened

0: Fast Role Swap has not happened

1: Fast Role Swap has happened

Bit 6 Unimplemented, read as “0”

Bit 5~3 **RX\_RESULT5~RX\_RESULT3**: Received status

000: No operation

001: Message Received - Read buffer

010: Hard reset from remote

011: Cable reset from remote

100~111: Reserved

Bit 2~0 **TX\_RESULT2~TX\_RESULT0**: Transmitter status

000: No operation

001: Message sent with success

010: Transmission error

011: Transmitter busy

100: Transmit discarded due to incoming message

101~111: Reserved

• **RX\_STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	RX_DATA	RX_OVERRUN	—	—	—	—	—	RX_CLEAR
R/W	RO	RO	—	—	—	—	—	WC
POR	0	0	—	—	—	—	—	0

Bit 7 **RX\_DATA**: Indicates buffer data is available

0: Buffer data is not available

1: Buffer data is available

- Bit 6      **RX\_OVERRUN**: New data has arrived without the previous data having been read  
           0: Read  
           1: Not read  
           Cleared by writing a “1” to RX\_CLEAR.
- Bit 5~1    Unimplemented, read as “0”
- Bit 0      **RX\_CLEAR**: Write a “1” to this bit to indicate data has been read  
           0: Reserved  
           1: Indicates data has been read  
           If there is another packet in buffer, RX\_DATA will remain 1.

● **RX\_INFO Register**

Bit	7	6	5	4	3	2	1	0
Name	RX_BYTES7	RX_BYTES6	RX_BYTES5	RX_BYTES4	RX_BYTES3	RX_SOP2	RX_SOP1	RX_SOP0
R/W	RO	RO	RO	RO	RO	RO	RO	RO
POR	0	0	0	0	0	0	0	0

- Bit 7~3    **RX\_BYTES7~RX\_BYTES3**: Actual number of bytes received
- Bit 2~0    **RX\_SOP2~RX\_SOP0**: SOP type of the received message  
           000: No Message  
           001: SOP  
           010: SOP'  
           011: SOP''  
           100: Debug SOP'  
           101: Debug SOP''  
           110~111: Reserved

● **TX\_COMMAND Register**

Bit	7	6	5	4	3	2	1	0
Name	TX_CMD7	TX_CMD6	TX_CMD5	—	—	TX_WAIT_RP	TX_START	TXBUF_READY
R/W	R/W	R/W	R/W	—	—	R/W	WC	RO
POR	0	0	0	—	—	0	0	1

- Bit 7~5    **TX\_CMD7~TX\_CMD5**: Transmit Commands control  
           000: NOP  
           001: Send the message in buffer  
           010: Send CableReset  
           011: Send HardReset  
           100: Start BIST Mode 2 for 45 ms  
           101~111: Unused
- Bit 4~3    Unimplemented, read as “0”
- Bit 2      **TX\_WAIT\_RP**: TX Wait R<sub>p</sub> control  
           0: TX does not wait  
           1: TX will hold until R<sub>p</sub> = 3 A
- Bit 1      **TX\_START**: A write to this bit starts transmission of what is in the TX buffer  
           0: Not transmission  
           1: Starts transmission

Bit 0 **TXBUF\_READY**: Transmission status  
 0: Transmission ongoing  
 1: Transmission complete  
 The software should check whether this bit is 1 before filling the transmit buffer.

• **TX\_INFO Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TX_RE- TRIES5	TX_RE- TRIES4	TX_RE- TRIES3	TX_ SOP2	TX_ SOP1	TX_ SOP0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	1	1	0	0	0

Bit 7~6 Unimplemented, read as “0”  
 Bit 5~3 **TX\_RETRIES5~TX\_RETRIES3**: Number of retries to be attempted for this message  
 Bit 2~0 **TX\_SOP2~TX\_SOP0**: SOP type of the transmitted message  
 000: Not Valid  
 001: SOP  
 010: SOP’  
 011: SOP’’  
 100: Debug SOP’  
 101: Debug SOP’’  
 110~111: Reserved

• **RX\_PACKET\_DATAm Register (m=61~90)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: Receive packet data  
 The SOP and EOP symbols are not included in the receive data. The first byte of the data is the 8 LSB’s of the packet header, and is ordered consistently with the power delivery specification. Also:

- The GoodCRC packets are consumed by the logic and do not appear in the receive buffer.
- The packet’s CRC is not included in the byte count. However, when space in the buffer is available, the CRC field appears after the data in the buffer.

• **TX\_PACKET\_DATA n Register (n=91~120)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: Transmit packet data  
 The SOP and EOP symbols are not included in the transmit data. The first byte of the data is the 8 LSB’s of the packet header, and is ordered consistently with the power delivery specification.

• **C\_OVP Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ENP2	ENP1	STP2	STP1
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as “0”

Bit 3~2 **ENP2~ENP1**: Associated Protect blocks enable control

- 00: Disable
- 01: CC1 Protect blocks enable
- 10: CC2 Protect blocks enable
- 11: CC1 and CC2 Protect blocks enable

The Protect blocks must be enabled before they are started.

Bit 1~0 **STP2~STP1**: Protect blocks for the associated CC1/CC2 Start control

- 00: Disable
- 01: CC1 OVP Start enable
- 10: CC2 OVP Start enable
- 11: CC1 and CC2 OVP Start enable

These can be started at boot time, or to save power only started when needed. The protect blocks must be first enabled with CC1/CC2 pin.

## PD PHY Reset

When the system is powered on for the first time, the SYSRESETN line needs to be sent a signal from low to high with a width of 30  $\mu$ s to complete the reset action. After this, send the I<sup>2</sup>C command to set the relevant registers.

## SVBUS External Divider Resistor Configuration

**Table 6. External Divider for 48 V EPR Scaled VBUS (SVBUS Input)**

Component	Connection	Note
220 k $\Omega$ + 680 $\Omega$ 1 % resistors	VBUS to SVBUS pin	—
12 k $\Omega$ + 1 k $\Omega$ 1 % resistors	SVBUS pin to ground	Good analog ground connection
10nF capacitor	SVBUS pin to ground	Good analog ground connection

## PD PHY I<sup>2</sup>C Function

The I<sup>2</sup>C serial interface is a two line interface, a serial data line, SDA\_PD, and serial clock line, SCL\_PD. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I<sup>2</sup>C bus is identified by a unique address which will be transmitted and received on the I<sup>2</sup>C bus. When two devices communicate with each other on the bidirectional I<sup>2</sup>C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus. For the device, which only operates in slave mode, there are two methods of transferring data on the I<sup>2</sup>C bus, the slave transmit mode and the slave receive mode.

Communication on the I<sup>2</sup>C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I<sup>2</sup>C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address, the 8th bit is the read/write bit

whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. The transmitted data is 8-bit wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8 bits of data, the receiver must transmit an acknowledge signal, level “0”, before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA\_PD line to allow the master to send a STOP signal to release the I<sup>2</sup>C Bus.

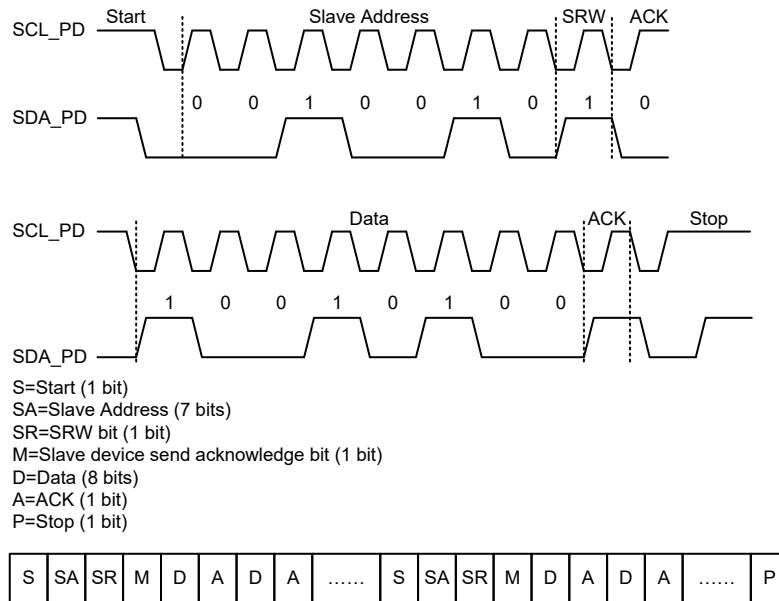


Figure 4. PD PHY I<sup>2</sup>C Communication Timing Diagram

### Device Addressing

The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is “1”, then a read operation is selected. A “0” selects a write operation. The device address bits are “0010010”. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA\_PD line.

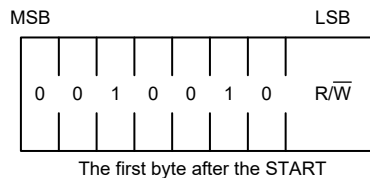


Figure 5. Device Addressing



## Write/Read Timing

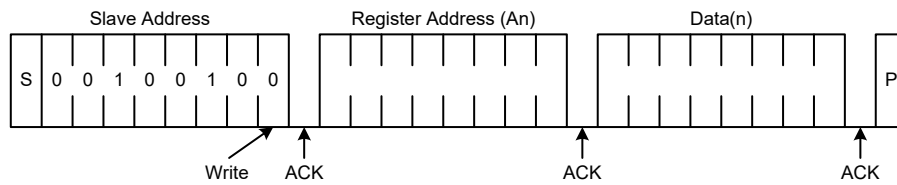


Figure 6. Byte Write Timing

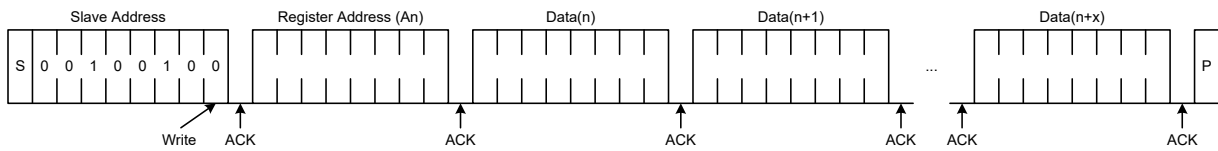


Figure 7. Page Write Timing

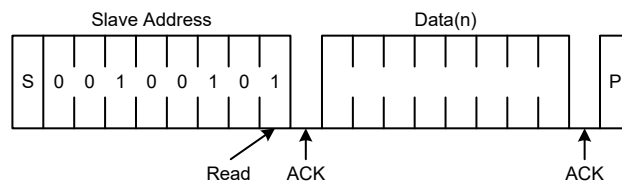


Figure 8. Read Timing

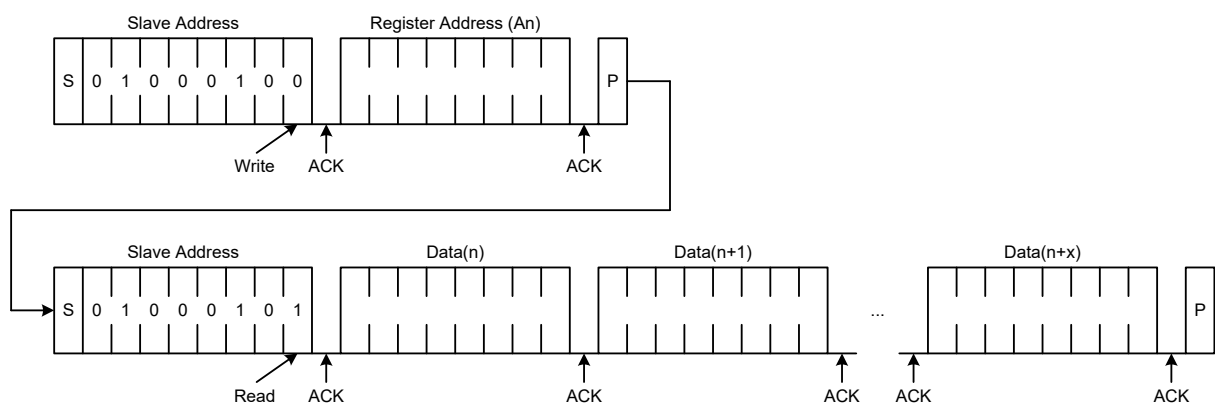


Figure 9. Random Read Timing

# 5 Pin Assignment

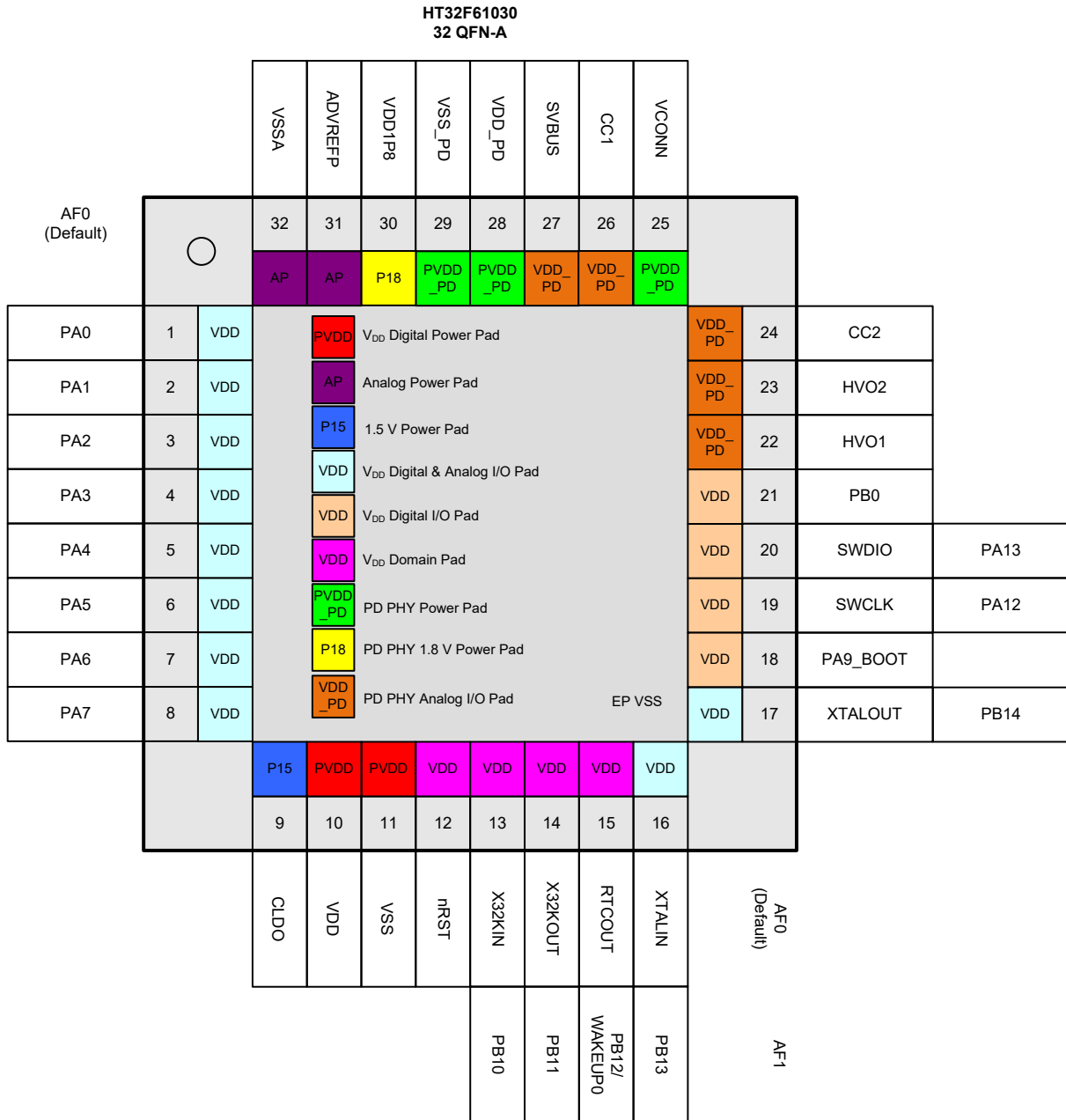


Figure 10. 32-pin QFN Pin Assignment

**Table 7. Pin Assignment**

Package	Alternate Function Mapping							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
<b>32QFN</b>	<b>System Default</b>	<b>System Other</b>	<b>ADC</b>	<b>N/A</b>	<b>SCTM</b>	<b>SPI</b>	<b>UART</b>	<b>I<sup>2</sup>C</b>
1	PA0	VBG	ADC_IN2		SCTM1_CH0	SPI_SCK		I2C_SCL
2	PA1		ADC_IN3		SCTM1_CH1	SPI_MOSI		I2C_SDA
3	PA2		ADC_IN4			SPI_MISO	UR0_TX	
4	PA3		ADC_IN5			SPI_SEL	UR0_RX	
5	PA4		ADC_IN6			SPI_SCK	UR1_TX	I2C_SCL
6	PA5		ADC_IN7			SPI_MOSI	UR1_RX	I2C_SDA
7	PA6		ADC_IN8			SPI_MISO		
8	PA7		ADC_IN9			SPI_SEL		
9	CLDO							
10	VDD							
11, EP*	VSS							
12	nRST							
13	X32KIN	PB10			SCTM1_CH1	SPI_SEL	UR1_TX	
14	X32KOUT	PB11			SCTM1_CH0	SPI_SCK	UR1_RX	
15	RTCOUT	PB12 / WAKEUP0			SCTM0_CH1	SPI_MISO		
16	XTALIN	PB13			SCTM2_CH0		UR0_TX	I2C_SCL
17	XTALOUT	PB14			SCTM2_CH1		UR0_RX	I2C_SDA
18	PA9_BOOT	CKOUT			SCTM1_CH0	SPI_MOSI		
19	SWCLK	PA12						
20	SWDIO	PA13						
21	PB0				SCTM2_CH0	SPI_MOSI	UR0_TX	I2C_SCL
22	HVO1							
23	HVO2							
24	CC2							
25	VCONN							
26	CC1							
27	SVBUS							
28	VDD_PD							
29	VSS_PD							
30	VDD1P8							
31	ADVREFP							
32	VSSA							

Note: The EP is meant the exposed pad of the QFN package.

**Table 8. Pin Description**

Pin Number 32QFN	Pin Name	Type <sup>(1)</sup>	I/O Structure <sup>(2)</sup>	Output Driving	Description
					Default Function (AF0)
1	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode
6	PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode
7	PA6	AI/O	5V	4/8/12/16 mA	PA6
8	PA7	AI/O	5V	4/8/12/16 mA	PA7
9	CLDO	P	—	—	Core power LDO output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS
10	VDD	P	—	—	Voltage for digital I/O
11, EP	VSS	P	—	—	Ground reference for digital I/O
12	nRST <sup>(3)</sup>	I	5V_PU	—	External reset
13	PB10 <sup>(3)</sup>	AI/O (V <sub>DD</sub> )	5V	4/8/12/16 mA	X32KIN
14	PB11 <sup>(3)</sup>	AI/O (V <sub>DD</sub> )	5V	4/8/12/16 mA	X32KOUT
15	PB12 <sup>(3)</sup>	I/O (V <sub>DD</sub> )	5V	4/8/12/16 mA	RTCOUT
16	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
17	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
18	PA9	I/O (V <sub>DD</sub> )	5V_PU	4/8/12/16 mA	PA9_BOOT
19	PA12	I/O (V <sub>DD</sub> )	5V_PU	4/8/12/16 mA	SWCLK
20	PA13	I/O (V <sub>DD</sub> )	5V_PU	4/8/12/16 mA	SWDIO
21	PB0	I/O (V <sub>DD</sub> )	5V	4/8/12/16 mA	PB0
22	HVO1	OD	—	—	Open drain output 1
23	HVO2	OD	—	—	Open drain output 2
24	CC2	AI/O	—	—	USB Type-C PD configuration channel 2
25	VCONN	P	—	—	VCONN power 3 V ~ 5.5 V input
26	CC1	AI/O	—	—	USB Type-C PD configuration channel 1

Pin Number	Pin Name	Type <sup>(1)</sup>	I/O Structure <sup>(2)</sup>	Output Driving	Description
					Default Function (AF0)
27	SVBUS	AI	—	—	USB VBUS connector
28	VDD_PD	PWR	—	—	PD PHY Positive power supply
29	VSS_PD	PWR	—	—	PD PHY Negative power supply, ground
30	VDD1P8	PWR	—	—	PD PHY Regulator output pin and 1.8 V Digital positive power supply
31	ADVREFP	P	—	—	Positive reference voltage for the ADC
32	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, OD = Open-Drain output, V<sub>DD</sub> = V<sub>DD</sub> Power, EP = Exposed Pad.

2. 5V = 5 V operation I/O type, PU = Pull-up.

3. These pins are located at the V<sub>DD</sub> power domain.

4. In the Boot loader mode, only the UART interface can be used for communication.

## Internal Connection Signal Lines

The MCU generated signals such as the I2C\_SCL have been internally connected to the power delivery for control purpose. The connections are listed in the following table and the related control registers should be configured correctly using application program.

**Table 9. Internal Connection Signal Lines**

MCU Signal Name	Connected PD PHY Signal Name	Description
PB7 / I2C_SCL (I <sup>2</sup> C)	SCL_PD	PD PHY I <sup>2</sup> C Clock line. The MCU AFIO setting should be AF7 to select the I <sup>2</sup> C pin function.
PB6 / I2C_SDA (I <sup>2</sup> C)	SDA_PD	PD PHY I <sup>2</sup> C data line. The MCU AFIO setting should be AF7 to select the I <sup>2</sup> C pin function.
PF0	HVI1	Open drain control logic 1. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PF1	HVI2	Open drain control logic 2. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PC2	SYSRESETN	PD PHY reset input signal. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PC3	BUS_INT	BUS interrupt output signal. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.

# 6 Application Circuits

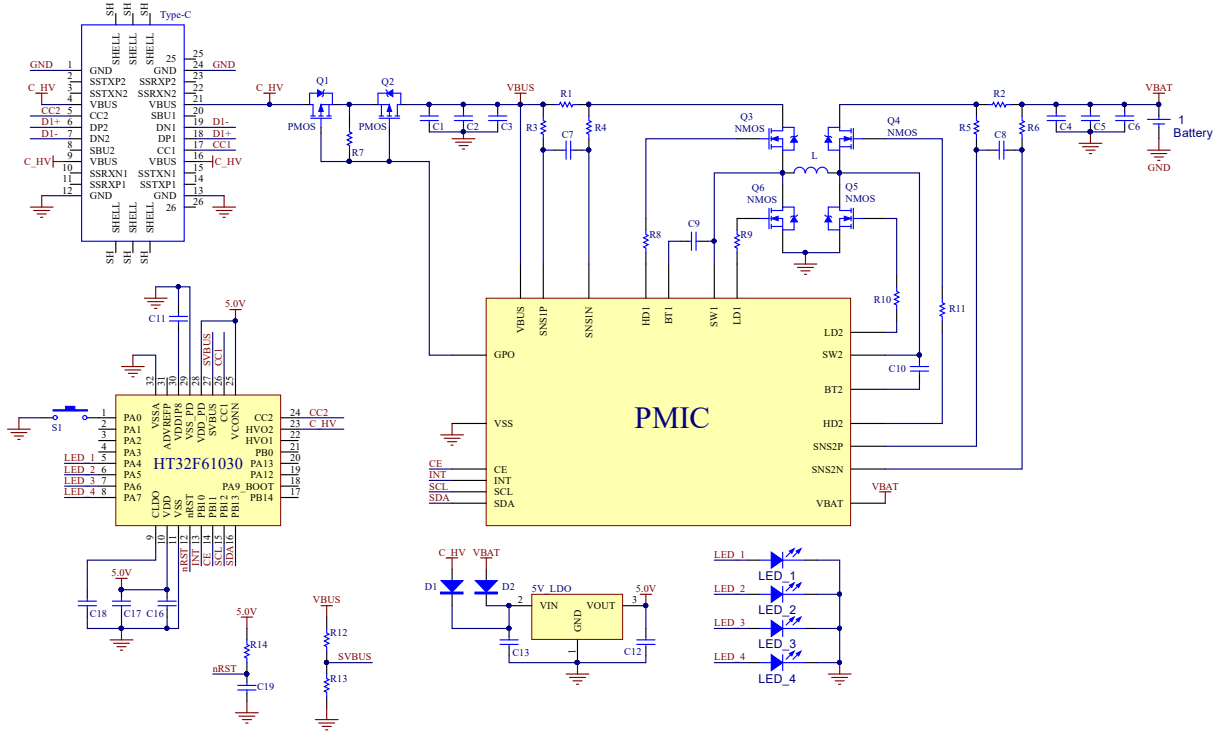


Figure 11. Application Circuit

# 7 Electrical Characteristics

## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 10. Absolute Maximum Ratings**

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	External Main Supply Voltage	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 5.5	V
V <sub>DDA</sub>	External Analog Supply Voltage	V <sub>SSA</sub> - 0.3	V <sub>SSA</sub> + 5.5	V
V <sub>IN</sub>	Input Voltage on I/O	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
T <sub>A</sub>	Ambient Operating Temperature Range	-40	85	°C
T <sub>STG</sub>	Storage Temperature Range	-60	150	°C
T <sub>J</sub>	Maximum Junction Temperature	—	125	°C
P <sub>D</sub>	Total Power Dissipation	—	500	mW

## Recommended DC Operating Conditions

**Table 11. Recommended DC Operating Conditions**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage	—	2.5	5.0	5.5	V
V <sub>ADVREFP</sub>	ADC Positive Reference Voltage	—	2.5	5.0	5.5	V

Note: The V<sub>ADVREFP</sub> power voltage needs below or equal to the V<sub>DD</sub> power voltage.

## On-Chip LDO Voltage Regulator Characteristics

**Table 12. LDO Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>LDO</sub>	Internal Regulator Output Voltage	V <sub>DD</sub> ≥ 2.5 V Regulator input @ I <sub>LDO</sub> = 12 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I <sub>LDO</sub>	Output Current	V <sub>DD</sub> = 2.5 V Regulator input @ V <sub>LDO</sub> = 1.5 V	—	12	15	mA
C <sub>LDO</sub>	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

## Power Consumption

Table 13. Power Consumption Characteristics

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	f <sub>HCLK</sub>	Conditions	Typ.	Max @ T <sub>A</sub>		Unit	
					25 °C	85 °C		
I <sub>DD</sub>	Supply Current (Run Mode)	16 MHz	V <sub>DD</sub> = 5 V HSI = 16 MHz	All peripherals enabled	3.35	3.60	—	mA
				All peripherals disabled	2.75	2.95	—	
		8 MHz	V <sub>DD</sub> = 5 V HSI = 16 MHz	All peripherals enabled	1.88	2.02	—	
				All peripherals disabled	1.57	1.69	—	
		32 kHz	V <sub>DD</sub> = 5 V LSI = 32 kHz LDO in LCM Mode	All peripherals enabled	26.39	32.72	—	μA
				All peripherals disabled	25.13	31.42	—	
	Supply Current (Sleep Mode)	16 MHz	V <sub>DD</sub> = 5 V HSI = 16 MHz	All peripherals enabled	1.16	1.24	—	mA
				All peripherals disabled	0.44	0.48	—	
		8 MHz	V <sub>DD</sub> = 5 V HSI = 16 MHz	All peripherals enabled	0.77	0.83	—	
				All peripherals disabled	0.41	0.45	—	
Supply Current (Deep-Sleep1 Mode)	—	V <sub>DD</sub> = 5 V, HSI/HSE clock off, LDO in LCM Mode, LSE off, LSI on, RTC on		20.27	26.39	—	μA	
Supply Current (Deep-Sleep2 Mode)	—	V <sub>DD</sub> = 5 V, HSI/HSE clock off, LDO off, DMOS on, LSE off, LSI on, RTC on		3.45	5.14	—	μA	

- Note: 1. HSE means high speed external oscillator. HSI means 16 MHz high speed internal oscillator.  
 2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.  
 3. RTC means real-time clock.  
 4. Code = while (1) { 208 NOP } executed in Flash.

## Reset and Supply Monitor Characteristics

Table 14. V<sub>DD</sub> Power Reset Characteristics

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>POR</sub>	Power On Reset Threshold (Rising Voltage on V <sub>DD</sub> )	T <sub>A</sub> = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V <sub>PDR</sub>	Power Down Reset Threshold (Falling Voltage on V <sub>DD</sub> )		2.12	2.2	2.33	V
V <sub>PORHYST</sub>	POR Hysteresis	—	—	150	—	mV
t <sub>POR</sub>	Reset Delay Time	V <sub>DD</sub> = 5.0 V	—	0.1	0.2	ms

- Note: 1. Data based on characterization results only, not tested in production.  
 2. If the LDO is turned on, the V<sub>DD</sub> POR has to be in the de-assertion condition. When the V<sub>DD</sub> POR is in the assertion state then the LDO will be turned off.



**Table 15. LVD / BOD Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V <sub>BOD</sub>	Voltage of Brown Out Detection	After factory-trimmed, V <sub>DD</sub> falling edge	2.37	2.45	2.53	V	
V <sub>LVD</sub>	Voltage of Low Voltage Detection	V <sub>DD</sub> falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
	LVDS = 111	4.55	4.65	4.75	V		
V <sub>LVDHTST</sub>	LVD Hysteresis	V <sub>DD</sub> = 5.0 V	—	—	100	mV	
t <sub>suLVD</sub>	LVD Setup Time	V <sub>DD</sub> = 5.0 V	—	—	5	μs	
t <sub>alLVD</sub>	LVD Active Delay Time	V <sub>DD</sub> = 5.0 V	—	—	—	ms	
I <sub>DDLVD</sub>	Operation Current <sup>(2)</sup>	V <sub>DD</sub> = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.

2. Bandgap current is not included.

3. LVDS field is in the PWRCU LVDCSR register.

## External Clock Characteristics

**Table 16. High Speed External Clock (HSE) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operation Range	T <sub>A</sub> = -40 °C ~ 85 °C	2.5	—	5.5	V
f <sub>HSE</sub>	HSE Frequency	V <sub>DD</sub> = 2.5 V ~ 5.0 V	4	—	16	MHz
C <sub>L</sub>	Load Capacitance	V <sub>DD</sub> = 5.0 V, R <sub>ESR</sub> = 100 Ω @ 16 MHz	—	—	12	pF
R <sub>FHSE</sub>	Internal Feedback Resistor between XTALIN and XTALOUT Pins	V <sub>DD</sub> = 5.0 V	—	0.5	—	MΩ
R <sub>ESR</sub>	Equivalent Series Resistance	V <sub>DD</sub> = 5.0 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	110	Ω
		V <sub>DD</sub> = 2.5 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEGAIN = 1	—	—	—	—
D <sub>HSE</sub>	HSE Oscillator Duty Cycle	—	40	—	60	%
I <sub>DDHSE</sub>	HSE Oscillator Current Consumption	V <sub>DD</sub> = 5.0 V, R <sub>ESR</sub> = 100 Ω, C <sub>L</sub> = 12 pF @ 8 MHz, HSEGAIN = 0	—	0.85	—	mA
		V <sub>DD</sub> = 5.0 V, R <sub>ESR</sub> = 25 Ω, C <sub>L</sub> = 12 pF @ 16 MHz, HSEGAIN = 1	—	3.0	—	
I <sub>PWDHSE</sub>	HSE Oscillator Power Down Current	V <sub>DD</sub> = 5.0 V	—	—	0.01	μA
t <sub>SUHSE</sub>	HSE Oscillator Startup Time	V <sub>DD</sub> = 5.0 V	—	—	4	ms

**Table 17. Low Speed External Clock (LSE) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operation Range	T <sub>A</sub> = -40 °C ~ 85 °C	2.5	—	5.5	V
f <sub>CK_LSE</sub>	LSE Frequency	V <sub>DD</sub> = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R <sub>F</sub>	Internal feedback resistor	—	—	10	—	MΩ
R <sub>ESR</sub>	Equivalent Series Resistance	V <sub>DD</sub> = 5.0 V	30	—	TBD	kΩ
C <sub>L</sub>	Recommended load capacitances	V <sub>DD</sub> = 5.0 V	6	—	TBD	pF
I <sub>DDLSE</sub>	Oscillator Supply Current (High Current Mode)	f <sub>CK_LSE</sub> = 32.768 kHz, R <sub>ESR</sub> = 50 kΩ, C <sub>L</sub> ≥ 7 pF V <sub>DD</sub> = 2.5 V ~ 5.5 V T <sub>A</sub> = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f <sub>CK_LSE</sub> = 32.768 kHz, R <sub>ESR</sub> = 50 kΩ, C <sub>L</sub> < 7 pF V <sub>DD</sub> = 2.5 V ~ 5.5 V T <sub>A</sub> = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t <sub>SULSE</sub>	LSE Oscillator Startup Time (Low Current Mode)	f <sub>CK_LSE</sub> = 32.768 kHz, V <sub>DD</sub> = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

## Internal Clock Characteristics

**Table 18. High Speed Internal Clock (HSI) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operation Range	T <sub>A</sub> = -40 °C ~ 85 °C	2.5	—	5.5	V
f <sub>HSI</sub>	HSI Frequency	V <sub>DD</sub> = 5 V @ 25 °C	—	16	—	MHz
ACC <sub>HSI</sub>	Factory Calibrated HSI Oscillator Frequency Accuracy	V <sub>DD</sub> = 2.5 V ~ 5.5 V, T <sub>A</sub> = 25 °C	-1	—	1	%
		V <sub>DD</sub> = 2.5 V ~ 5.5 V T <sub>A</sub> = -25 °C ~ 85 °C	-2.5	—	2	%
		V <sub>DD</sub> = 2.5 V ~ 5.5 V T <sub>A</sub> = -40 °C ~ 85 °C	-4	—	3	%
Duty	Duty Cycle	f <sub>HSI</sub> = 16 MHz	35	—	65	%
I <sub>DDHSI</sub>	Oscillator Supply Current	f <sub>HSI</sub> = 16 MHz	—	—	140	μA
	Power Down Current	@ V <sub>DD</sub> = 2.5 V ~ 5.5 V	—	—	0.01	μA
T <sub>SUHSI</sub>	HSI Oscillator Startup Time	f <sub>HSI</sub> = 16 MHz	—	—	20	μs

**Table 19. Low Speed Internal Clock (LSI) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operation Range	T <sub>A</sub> = -40 °C ~ 85 °C	2.5	—	5.5	V
f <sub>LSI</sub>	LSI Frequency	V <sub>DD</sub> = 5.0 V, T <sub>A</sub> = -40 °C ~ 85 °C	21	32	43	kHz
ACC <sub>LSI</sub>	LSI Frequency Accuracy	V <sub>DD</sub> = 5.0 V, with factory-trimmed	-10	—	+10	%
I <sub>DDLSI</sub>	LSI Oscillator Operating Current	V <sub>DD</sub> = 5.0 V	—	0.5	0.8	µA
t <sub>SULSI</sub>	LSI Oscillator Startup Time	V <sub>DD</sub> = 5.0 V	—	—	100	µs

## Memory Characteristics

**Table 20. Flash Memory Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N <sub>ENDU</sub>	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T <sub>A</sub> = -40 °C ~ 85 °C	20	—	—	K cycles
t <sub>RET</sub>	Data Retention Time	T <sub>A</sub> = -40 °C ~ 85 °C	10	—	—	Years
t <sub>PROG</sub>	Word Programming Time	T <sub>A</sub> = -40 °C ~ 85 °C	20	—	—	µs
t <sub>ERASE</sub>	Page Erase Time	T <sub>A</sub> = -40 °C ~ 85 °C	2	—	—	ms
t <sub>MERASE</sub>	Mass Erase Time	T <sub>A</sub> = -40 °C ~ 85 °C	10	—	—	ms

## I/O Port Characteristics

**Table 21. I/O Port Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I <sub>IL</sub>	Low Level Input Current	5.0 V I/O	V <sub>I</sub> = V <sub>SS</sub> , On-chip pull-up resistor disabled	—	—	3	µA
		Reset pin		—	—	3	µA
I <sub>IH</sub>	High Level Input Current	5.0 V I/O	V <sub>I</sub> = V <sub>DD</sub> , On-chip pull-down resistor disabled	—	—	3	µA
		Reset pin		—	—	3	µA
V <sub>IL</sub>	Low Level Input Voltage	5.0 V I/O		-0.5	—	V <sub>DD</sub> × 0.35	V
		Reset pin		-0.5	—	V <sub>DD</sub> × 0.35	V
V <sub>IH</sub>	High Level Input Voltage	5.0 V I/O		V <sub>DD</sub> × 0.65	—	V <sub>DD</sub> + 0.5	V
		Reset pin		V <sub>DD</sub> × 0.65	—	V <sub>DD</sub> + 0.5	V
V <sub>HYS</sub>	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V <sub>DD</sub>	—	mV
		Reset pin		—	0.12 × V <sub>DD</sub>	—	mV
I <sub>OL</sub>	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V <sub>OL</sub> = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V <sub>OL</sub> = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V <sub>OL</sub> = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V <sub>OL</sub> = 0.6 V		16	—	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.6 V	—	4	—	mA
		5.0 V I/O 8 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.6 V	—	8	—	mA
		5.0 V I/O 12 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.6 V	—	12	—	mA
		5.0 V I/O 16 mA drive, V <sub>OH</sub> = V <sub>DD</sub> - 0.6 V	—	16	—	mA
V <sub>OL</sub>	Low Level Output Voltage	5.0 V 4 mA drive I/O, I <sub>OL</sub> = 4 mA	—	—	0.6	V
		5.0 V 8 mA drive I/O, I <sub>OL</sub> = 8 mA	—	—	0.6	V
		5.0 V 12 mA drive I/O, I <sub>OL</sub> = 12 mA	—	—	0.6	V
		5.0 V 16 mA drive I/O, I <sub>OL</sub> = 16 mA	—	—	0.6	V
V <sub>OH</sub>	High Level Output Voltage	5.0 V 4 mA drive I/O, I <sub>OH</sub> = 4 mA	V <sub>DD</sub> - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I <sub>OH</sub> = 8 mA	V <sub>DD</sub> - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I <sub>OH</sub> = 12 mA	V <sub>DD</sub> - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I <sub>OH</sub> = 16 mA	V <sub>DD</sub> - 0.6	—	—	V
R <sub>PU</sub>	Internal Pull-up Resistor	V <sub>DD</sub> = 5.0 V	—	50	—	kΩ
R <sub>PD</sub>	Internal Pull-down Resistor	V <sub>DD</sub> = 5.0 V	—	50	—	kΩ

## ADC Characteristics

Table 22. ADC Characteristics

T<sub>A</sub> = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Operating Voltage	—	2.5	5.0	5.5	V
V <sub>ADCIN</sub>	A/D Converter Input Voltage Range	—	0	—	V <sub>REF+</sub>	V
V <sub>REF+</sub>	A/D Converter Positive Reference Voltage	—	—	—	V <sub>DDA</sub>	V
I <sub>ADC</sub>	Current Consumption	V <sub>DDA</sub> = 5.0 V, 500 ksps	—	1.4	1.5	mA
I <sub>ADC_DN</sub>	Power Down Current Consumption	V <sub>DDA</sub> = 5.0 V	—	—	0.1	μA
f <sub>ADC</sub>	A/D Converter Clock Frequency	—	0.7	—	8	MHz
f <sub>S</sub>	Sampling Rate	—	50	—	500	ksps
t <sub>DL</sub>	Data Latency	—	—	12.5	—	1/f <sub>ADC</sub> Cycles
t <sub>S&amp;H</sub>	Sampling & Hold Time	—	—	3.5	—	1/f <sub>ADC</sub> Cycles
t <sub>ADCCONV</sub>	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	1/f <sub>ADC</sub> Cycles
R <sub>I</sub>	Input Sampling Switch Resistance	—	—	—	1	kΩ
C <sub>I</sub>	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t <sub>SU</sub>	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	Bits
INL	Integral Non-linearity Error	f <sub>S</sub> = 500 ksps, V <sub>DDA</sub> = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f <sub>S</sub> = 500 ksps, V <sub>DDA</sub> = 5.0 V	—	±1	—	LSB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E <sub>O</sub>	Offset Error	—	—	—	±10	LSB
E <sub>G</sub>	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C<sub>1</sub> is the storage capacitor, R<sub>1</sub> is the resistance of the sampling switch and R<sub>S</sub> is the output impedance of the signal source V<sub>S</sub>. Normally the sampling phase duration is approximately, 3.5/f<sub>ADC</sub>. The capacitance, C<sub>1</sub>, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V<sub>S</sub> for accuracy. To guarantee this, R<sub>S</sub> is not allowed to have an arbitrarily large value.

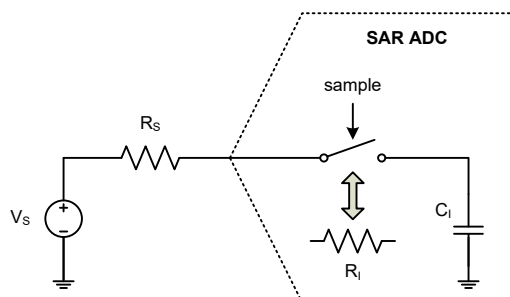


Figure 12. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V<sub>REF+</sub>) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_1 \ln(2^{N+2})} - R_1$$

Where f<sub>ADC</sub> is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R<sub>S</sub> may be larger than the value indicated by the equation above.

## Internal Reference Voltage Characteristics

Table 23. Internal Reference Voltage Characteristics

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Operating Voltage	—	2.8	—	5.5	V
V <sub>REF</sub>	Internal Reference Voltage after Factory Trimming, @ T <sub>A</sub> = 25 °C	V <sub>DDA</sub> ≥ 2.8 V VREFSEL[1:0] = 00	2.44	2.50	2.56	V
		V <sub>DDA</sub> ≥ 3.3 V VREFSEL[1:0] = 01	2.92	3.00	3.08	
		V <sub>DDA</sub> ≥ 4.3 V VREFSEL[1:0] = 10	3.90	4.00	4.10	
		V <sub>DDA</sub> ≥ 4.8 V VREFSEL[1:0] = 11	4.39	4.50	4.61	
ACC <sub>VREF</sub>	Reference Voltage Accuracy after Trimming	V <sub>DDA</sub> = 2.8 V ~ 5.5 V, V <sub>REF</sub> = 2.5 V, T <sub>A</sub> = -40 °C ~ 85 °C	-2	—	+2	%
t <sub>STABLE</sub>	Reference Voltage Stable Time	—	—	—	100	ms
t <sub>SREFV</sub>	ADC Sampling Time when Reading Reference Voltage	—	10	—	—	µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD}$	Operating Current	—	—	50	70	$\mu\text{A}$
$I_{DDPWD}$	Power Down Current	—	—	—	0.01	$\mu\text{A}$

Note: 1. Data based on characterization results only, not tested in production.  
2. The trimming bits of the internal reference voltage are 7-bit resolution.

## SCTM Characteristics

Table 24. SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{TM}$	Timer Clock Source for SCTM	—	—	—	$f_{PCLK}$	MHz
$t_{RES}$	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
$f_{EXT}$	External Signal Frequency on Channel	—	—	—	1/2	$f_{TM}$
RES	Timer Resolution	—	—	—	16	Bits

## PD PHY Characteristics

### PD PHY Operating Voltage Characteristics

Table 25. PD PHY Operating Voltage Characteristics

$T_A = -40\text{ }^\circ\text{C} \sim 85\text{ }^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD\_PD}$	Operating Voltage	—	2.6	—	5.5	V

### PD PHY Operating Current Characteristics

Table 26. PD PHY Operating Current Characteristics

$T_A = -40\text{ }^\circ\text{C} \sim 85\text{ }^\circ\text{C}$

Symbol	Operating Mode	Conditions	Min.	Typ.	Max.	Unit
$I_{DD\_PD}$	Normal Mode	$V_{DD\_PD} = 3\text{ V}, PWR[3:0] = 0xD$	—	1.5	3	mA
		$V_{DD\_PD} = 5\text{ V}, PWR[3:0] = 0xD$	—	2	5	mA
	SLEEP1 Mode	$V_{DD\_PD} = 3\text{ V}, PWR[3:0] = 0x2$	—	10	20	$\mu\text{A}$
		$V_{DD\_PD} = 5\text{ V}, PWR[3:0] = 0x2$	—	20	60	$\mu\text{A}$
	SLEEP0 Mode	$V_{DD\_PD} = 3\text{ V}, PWR[3:0] = 0x0$	—	3	6	$\mu\text{A}$
		$V_{DD\_PD} = 5\text{ V}, PWR[3:0] = 0x0$	—	5	45	$\mu\text{A}$

### PD PHY LDO Characteristics

Table 27. PD PHY LDO Characteristics

$V_{DD\_PD} = V_{IN}, V_{IN} = V_{OUT} + 0.8\text{ V}, C_{LOAD} = 4.7\text{ }\mu\text{F}, T_A = -40\text{ }^\circ\text{C} \sim 85\text{ }^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD\_PD}$	Supply Voltage	—	2.6	—	5.5	V
$V_{OUT}$	Output Voltage	$T_A = 25\text{ }^\circ\text{C}, I_{LOAD} = 0.5\text{ mA}$	-4%	1.8	4%	V
		$I_{LOAD} = 0.5\text{ mA}$	-8%	1.8	8%	V
$I_Q$	Quiescent Current	$V_{DD\_PD} = 5\text{ V}$ , No load	—	—	10	$\mu\text{A}$
$I_{OUT}$	Output Current	$V_{IN} = 2.6\text{ V}, \Delta V_{OUT} = 0.15\text{ V}, V_{OUT} = 1.8\text{ V}$	5	—	—	mA
TC	Temperature Coefficient	$I_{LOAD} = 5\text{ mA}$	—	$\pm 1.5$	$\pm 2$	mV/ $^\circ\text{C}$

## PD PHY HVO Characteristics

Table 28. PD PHY HVO Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Sink Current for HVO1, HVO2 Pins	$V_{DD\_PD} = 5\text{ V}$ , $V_{OL} = 0.1 V_{DD\_PD}$	20	35	—	mA

## PD PHY Characteristics

Table 29. PD PHY Characteristics

$T_A = -40\text{ °C} \sim 85\text{ °C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{VCONN}$	VCONN Voltage	—	3	—	5.5	V
$V_{CCOVP}$	CC1, CC2 Over Voltage Protection	—	-6%	$V_{DD\_PD}$	5%	V
$I_{AVDD}$	AVDD Current while Waiting to Receive	—	—	35	—	$\mu\text{A}$
$I_{RX}$	AVDD Current while Receiving	CDR_SELECT = 0	—	250	—	$\mu\text{A}$
$I_{TX}$	AVDD Current while Transmitting	—	—	—	1.5	mA
$I_{CC1LK}$	CC1 Pins Leakage Current	—	—	—	5	$\mu\text{A}$
$I_{CC2LK}$	CC2 Pins Leakage Current	—	—	—	5	$\mu\text{A}$
$V_{REF}$	DAC Reference Voltage	—	2.5	2.6	2.7	V
$N_R$	DAC Resolution	—	—	6	—	Bit
$V_{DAC}$	DAC Threshold	DAC[5:0] = 000000b ~ 111111b	-60	—	+40	mV
$V_{SLC2}$	Upper Slice Voltage Comparator Reference	—	800	850	880	mV
$V_{SLC1}$	Middle Slice Voltage Comparator Reference	—	520	550	590	mV
$V_{SLC0}$	Lower Slice Voltage Comparator Reference	—	220	250	280	mV
$T_{SLCT}$	Slice Analog Activity Test Timer Time	—	15	—	35	$\mu\text{s}$
$V_{TH3}$	3 A CC Detect Threshold	—	1.12	1.16	1.25	V
$V_{TH1P5}$	1.5 A CC Detect Threshold	—	580	610	640	mV
$V_{TH\_DEF}$	Default Current CC Detect Threshold	—	160	200	250	mV
$V_{RDTH330}$	$R_D$ Voltage Threshold for 330 $\mu\text{A}$ Pull Up	—	1.9	2.4	2.7	V
$V_{RDTH180}$	$R_D$ Voltage Threshold for 180 $\mu\text{A}$ Pull Up	—	1.5	1.6	1.7	V
$V_{RDTH80}$	$R_D$ Voltage Threshold for 80 $\mu\text{A}$ Pull Up	—	1.5	1.6	1.7	V
$V_{RATH330}$	$R_A$ Voltage Threshold for 330 $\mu\text{A}$ Pull Up	—	760	800	830	mV
$V_{RATH180}$	$R_A$ Voltage Threshold for 180 $\mu\text{A}$ Pull Up	—	280	320	420	mV
$V_{RATH80}$	$R_A$ Voltage Threshold for 80 $\mu\text{A}$ Pull Up	—	180	200	225	mV
$f_{I2C}$	I <sup>2</sup> C Clock Frequency	—	400	—	1000	kHz

## PD PHY Power on Reset Characteristics

Table 30. PD PHY Power on Reset Characteristics

$T_A = -40\text{ °C} \sim 85\text{ °C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR\_PD}$	$V_{DD\_PD}$ Start Voltage to Ensure Power-on Reset	—	—	—	100	mV
$RR_{POR\_PD}$	$V_{DD\_PD}$ Rising Rate to Ensure Power-on Reset	—	0.035	—	—	V/ms
$t_{POR\_PD}$	Minimum Time for $V_{DD\_PD}$ Stays at $V_{POR\_PD}$ to Ensure Power-on Reset	—	1	—	—	ms

## I<sup>2</sup>C Characteristics

Table 31. I<sup>2</sup>C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>SCL</sub>	SCL Clock Frequency	—	100	—	400	—	1000	kHz
t <sub>SCL(H)</sub>	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
t <sub>SCL(L)</sub>	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t <sub>FALL</sub>	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t <sub>RISE</sub>	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
t <sub>SU(SDA)</sub>	SDA Data Setup Time	500	—	125	—	50	—	ns
t <sub>H(SDA)</sub>	SDA Data Hold Time <sup>(5)</sup>	0	—	0	—	0	—	ns
	SDA Data Hold Time <sup>(6)</sup>	—	1.6	—	0.475	—	0.25	μs
t <sub>VD(SDA)</sub>	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
t <sub>SU(STA)</sub>	START Condition Setup Time	500	—	125	—	50	—	ns
t <sub>H(STA)</sub>	START Condition Hold Time	0	—	0	—	0	—	ns
t <sub>SU(STO)</sub>	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.

3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.

4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 16 MHz.

5. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.

6. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

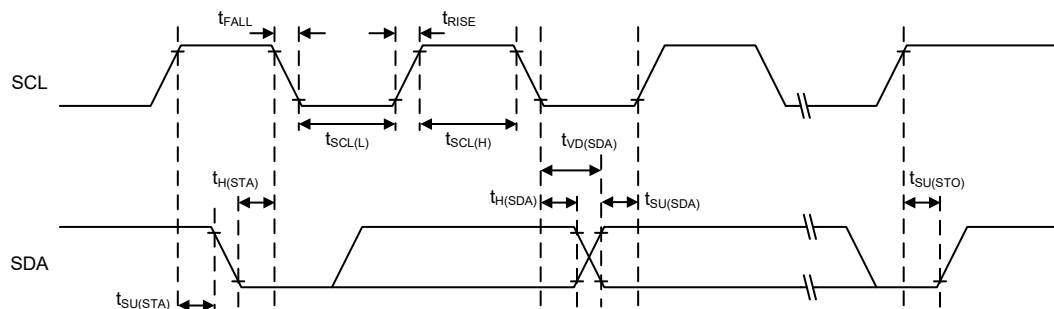


Figure 13. I<sup>2</sup>C Timing Diagram



## SPI Characteristics

**Table 32. SPI Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>SPI Master Mode</b>						
$f_{SCK}$	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency $f_{PCLK}$	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
<b>SPI Slave Mode</b>						
$f_{SCK}$	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency $f_{PCLK}$	—	—	$f_{PCLK}/3$	MHz
Duty <sub>SCK</sub>	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1.  $f_{SCK}$  is SPI output/input clock frequency and  $t_{SCK} = 1/f_{SCK}$ .

2.  $f_{PCLK}$  is SPI peripheral clock frequency and  $t_{PCLK} = 1/f_{PCLK}$ .

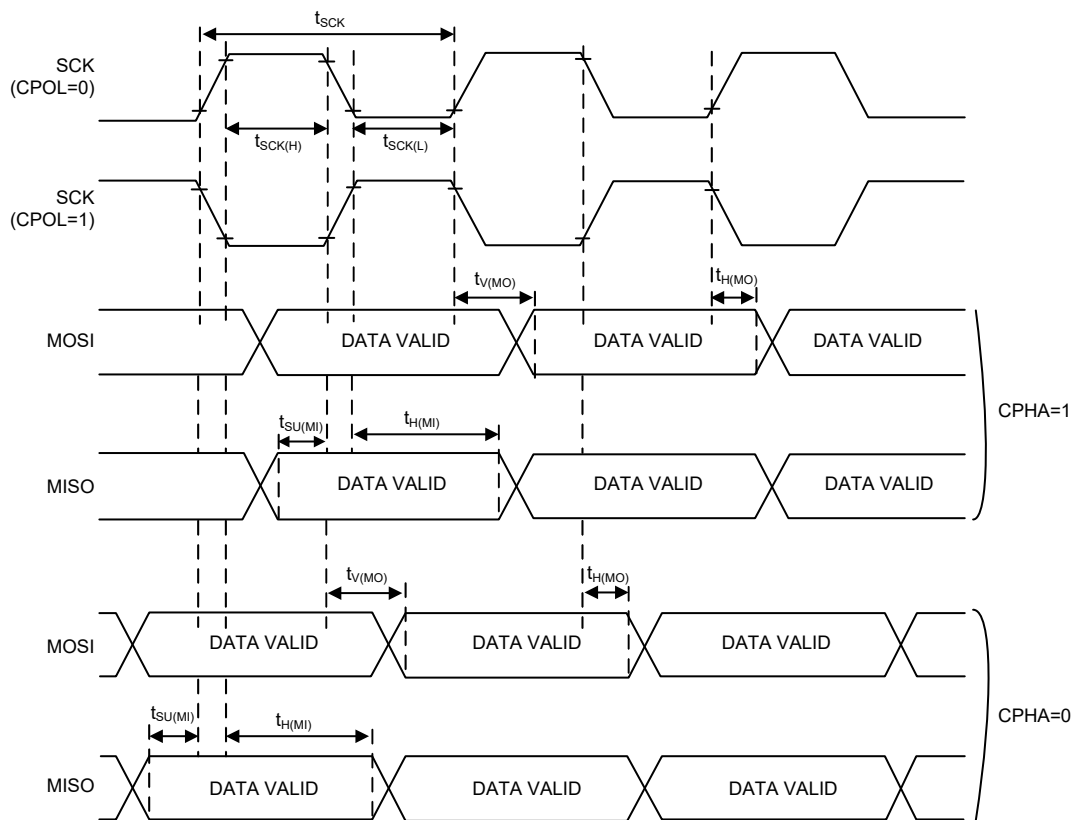


Figure 14. SPI Timing Diagram – SPI Master Mode

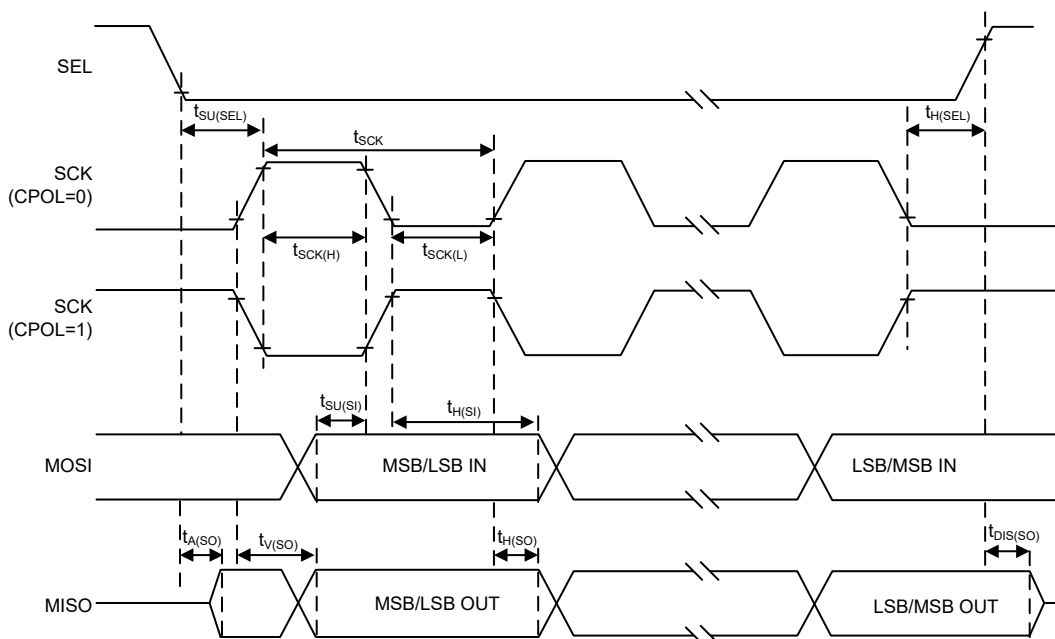


Figure 15. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

## 8 Package Information

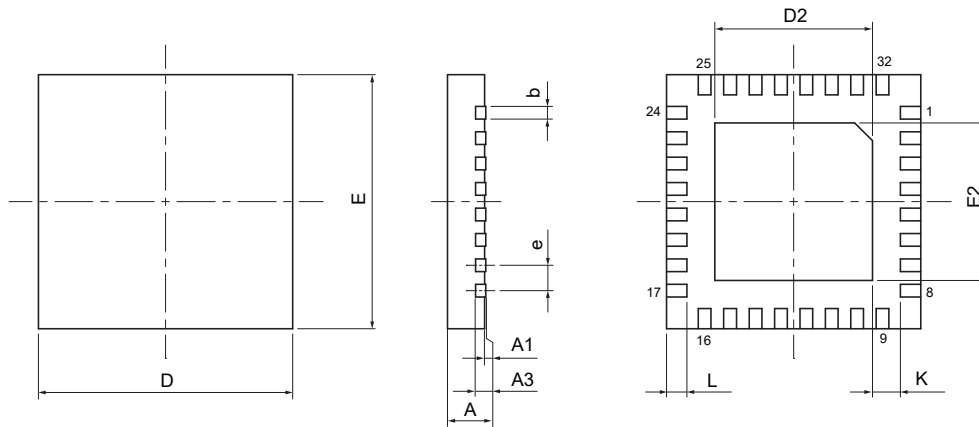
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- [Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [The Operation Instruction of Packing Materials](#)
- [Carton information](#)

## SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	0.008 REF		
b	0.006	0.008	0.010
D	0.157 BSC		
E	0.157 BSC		
e	0.016 BSC		
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.35	0.40	0.45
K	0.20	—	—

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