Using the Battery Voltage Detect Function in the HT45F4630

D/N: AN0423E

Introduction

The HT45F4630 contains a low voltage detect function, also known as the LVD. This allows the device to monitor the power supply voltage, VDD, or the external battery voltage, VCC, and provides a warning signal should it fall below a certain level. This function may be especially useful in battery applications, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

Functional Description

The Demo Board power supply circuit is shown below, where VCC1 stands for the external battery power supply and VDD is the LDO output voltage.

![VCC1 and VDD power supply circuit diagram]

Operating Principle

$V_{CC}$ Voltage Detection

The device provides a high voltage power supply detect circuit. The VCC1 power supply detect function is enabled or disabled using the EN_VDET bit. This detect circuit can output a power supply divided voltage using a resistor divider circuit. The divided voltage, $V_{DET}$, can also be read by connecting it to the A/D converter via the input channel AN5.
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VCC1 Power Supply Detect Circuit

VDD Voltage Detection

The Low Voltage Detector function operates by comparing the power supply voltage, VDD, with a pre-specified voltage level stored in the LVDC register. This has a range of between 2.0V and 4.0V. When the power supply voltage, VDD, falls below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. When the device is in the SLEEP mode, the low voltage detector will be disabled even if the ENLVD bit is high. After enabling the Low Voltage Detector, a time delay tLVDS should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the VDD voltage may rise and fall rather slowly, when the voltage approaches the VLVD voltage there may be multiple LVDO bit transitions.

LVD Operation

The Low Voltage Detector also has its own interrupt, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of tLVD after the LVDO bit has been set high by a low voltage condition. In this case, the LVDF interrupt request flag will be set, causing an interrupt to be generated if VDD falls below the preset LVD voltage. This will cause the device to wake-up, however if the Low Voltage Detector wake up function is not required then the LVDF flag should be first set high before the device enters the IDLE Mode. Note that the LVD function will be automatically disabled if the device enters the SLEEP Mode.
Battery Voltage Detection Usage

\textbf{V_{CC} voltage detection registers}

Step1: Enable the high voltage power supply detection function using the EN_VDET bit.

Step2: Select the required A/D conversion clock by correctly programming bits SACKS2~SACKS0 in the SADC1 register.

Step3: Enable the A/D converter by setting the ENADC bit in the SADC0 register to one.

Step4: Select AN5 as A/D input by setting the SACS3 ~ SACS0 bits in the SADC0 register to “0101”.

Step5: Select A/D converter data format by setting the ADRFS bit in the SADC0 register.
   0: A/D converter data format → SADOH = D[11:4]; SADOL = D[3:0]
   1: A/D converter data format → SADOH = D[11:8]; SADOL = D[7:0]

Step6: Select the reference voltage source by configuring the SAVRS1 ~ SAVRS0 bits in the SADC1 register.

Step7: If the A/D conversion interrupt is used, the global control bit, EMI, and the A/D converter interrupt enable bit, ADE, must both be set high in advance.

Step8: The A/D conversion procedure can now be initiated by setting the START bit in the SADC0 register from low to high and then low again.

Step9: To check when the analog to digital conversion process is complete, the EOCB bit in the SADC0 register can be polled. The A/D data registers SADOL and SADOH can be read to obtain the conversion value when the conversion is completed.
   EOCB bit 0: A/D conversion ended
   EOCB bit 1: A/D conversion in progress

Note1: When checking for the end of the conversion process, if the method of polling the EOCB bit in the SADC0 register is used, the interrupt enable step above can be omitted.

Note2: As the registers for V_{CC} voltage detection have no voltage choice, users should convert the value read by A/D converter to set the required voltage.
**V_DD Voltage Detect Register**

The Low Voltage Detector function is controlled using a single register with the name LVDC, which can be used to select one of eight fixed voltages below which a low voltage condition will be determined. The bit LVDO is an output flag for low voltage detection. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the V_DD voltage is above the preset low voltage value.

**Step1:** Enable the LVD function by setting the bit ENLVD high.

The ENLVD bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuit.

**Step2:** Enable the Bandgap voltage output control by setting the bit VBGEN to one.

The VBGEN bit is used to control the internal Bandgap reference voltage. If any of the ENLVD and VBGEN bits are set high, then the Bandgap reference voltage will be enabled. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

**Step3:** Select LVD voltage using the VLVD2~VLVD0 bits

<table>
<thead>
<tr>
<th>Code</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>2.0V</td>
</tr>
<tr>
<td>001</td>
<td>2.2V</td>
</tr>
<tr>
<td>010</td>
<td>2.4V</td>
</tr>
<tr>
<td>011</td>
<td>2.7V</td>
</tr>
<tr>
<td>100</td>
<td>3.0V</td>
</tr>
<tr>
<td>101</td>
<td>3.3V</td>
</tr>
<tr>
<td>110</td>
<td>3.6V</td>
</tr>
<tr>
<td>111</td>
<td>4.0V</td>
</tr>
</tbody>
</table>
**Conclusion**

This application note has shown the battery voltage detection operating principles and usage in the HT45F4630. Program examples are also provided to help users to understand how to use the HT45F4630 function quickly.

**Program Examples**

- VCC Voltage Detection.zip
- LVD_VDD.zip

**Versions and Modify Information**

<table>
<thead>
<tr>
<th>Date</th>
<th>Author</th>
<th>Issue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016.02.24</td>
<td>王子齊</td>
<td>First Version</td>
</tr>
</tbody>
</table>

**Reference Files**

Reference file: HT45F4630 Data Sheet

For more information, refer to the Holtek’s official website [www.holtek.com](http://www.holtek.com).
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