Using the 24-bit ΔΣ A/D Converter in the HT67F56xx

D/N: AN0416E

Introduction

Holtek has a range of 24-bit Delta Sigma A/D converter and LCD type Flash MCUs, one of which is the HT67F5650. The internal Delta Sigma A/D converter has an effective number of bits (ENOB) of up to 18. With its abundant hardware resources and flexible functions, the device will be highly capable of providing MCU solutions for a huge variety of high-precision measurement applications such as forehead thermometers, ear thermometers and high resolution electronic scales as well as other consumer products. The following provides a description of how to use the 24-bit ΔΣ A/D converter function.

Functional Description

The device contains a high accuracy multi-channel 24-bit delta-sigma analog-to-digital converter (ΔΣ A/D) and a programmable gain amplifier (PGA). Using the PGA function, the user can setup the best gain combination for the desired input signal amplification to be applied to the input signal of the 24-bit A/D converter.

The following block diagram illustrates the 24-bit A/D converter basic function. The signal input from the external channel is first amplified by the PGA and then enters the 24-bit A/D converter. After conversion, the ΔΣ A/D converter modulator will output 1-bit converted data to a SINC filter which can transform the 1-bit data into 24 bits.
Operating Principles

ENOB

The clock frequency, f_{ADCK}, determines the single bit data output rate of the 24-bit ADC. The FLMS[2:0] bits together with the selected over sampling rate, abbreviated to OSR, determine how many bits need to be sampled for data conversion. With a lower data rate, the resolution can be higher. But it will take more time to complete the A/D conversion. The following tables show the relationship between the data rate value and the obtained maximum effective resolution. For example, with a Data Rate set as 5Hz, this will give a maximum effective resolution of 19.7 bits while with a Data Rate set as 1600Hz will provide the highest conversion speed, but the maximum effective resolution will only be 14.5 bits.

Calculating the Data Rate

The 24-bit ADC data rate can be calculated using the equation below:

Data Rate = ADC clock / ADOR[2:0]

ADC Clock : f_{ADCK} = f_{MCLK} / FLMS[2:0]

f_{MCLK} = f_{SYS} / 2 / (ADCK[4:0] + 1)  (When set ADCK [4:0] = 0x1F, f_{MCLK} = f_{SYS})

For example, if a data rate of 10Hz is required and the selected HIRC oscillator frequency is 4.9152MHz,

Set ADCK [4:0] = 0x1F to let f_{MCLK} = f_{SYS}.
Set FLMS[2:0] = 000b to let f_{MCLK} / (30 x 2),
Set ADOR[2:0] = 001b to select OSR = 8192.

Thus the Data Rate = 4.9152MHz / (30 x 2 x 8192) = 10Hz.
Data Conversion

The full-scale converted digitised value of the 24-bit A/D converter is from 8388607 to -8388608 when written as a decimal value. The converted data format is formed by a two’s complement binary value. The MSB of the converted data is the signed bit. Since the full-scale analog input value is equal to the \( V_{CM} \) or the \( V_{REF} \) voltage, this gives a single bit analog input value equal to the differential reference voltage divided by 8388608.

\[
1 \text{ LSB} = \frac{\Delta V_{REF}}{8388608}
\]

1. The converted data of the input voltage through the 24-bit A/D converter can be calculated using the following formulas:

\[
\Delta S_I = (\text{PGAGN} \times \text{AGDN} \times \Delta D) + \text{DCSET}
\]

\[
\Delta V_{REF} = V_{REGN} \times \Delta V_{REF}
\]

24-bit ADC Conversion Data: \( \left( \frac{\Delta S_I}{\Delta V_{REF}} \right) \times 8388608 \)

- \( \Delta S_I \): Differential input signal after amplification and offset calculation
- \( \text{PGAGN} \): PGA gain
- \( \text{ADGN} \): 24-bit ADC gain
- \( \Delta D \): Differential input signal
- \( \text{DCSET} \): Offset voltage
- \( \Delta V_{REF} \): Differential reference input voltage after amplification
- \( V_{REGN} \): Reference voltage gain
- \( \Delta V_{REF} \): Reference voltage

2. The converted data can be recovered to a voltage value using the following formulas:

- If \( \text{MSB} = 0 \), Input Voltage =

\[
\frac{(Covetted\_data) \times \text{LSB-DCSET}}{\text{PGA} \times \text{ADGN}}
\]

- If \( \text{MSB} = 1 \), Input Voltage =

\[
\frac{(2's\_of\_Covetted\_data) \times \text{LSB} - \text{DCSET}}{\text{PGA} \times \text{ADGN}}
\]
24-bit A/D Converter Settings and Usage Steps

A/D Converter Settings
Step 1: Enable the LDO and the VCM to provide a voltage for the PGA and ADC using the PWRC register.
Step 2: Select the PGA, ADC and ADC reference gain using the PGAC0 register.
Step 3: Setup the PGA input pin connection and the VCM voltage using the PGAC1 register.
Step 4: Select the PGA input channels using the PGACS register.
Step 5: Set the ADCK[4:0] bits in the ADCS register to select the required ADC clock frequency, \( f_{MCLK} \).
Step 6: Setup the output data rate.

\[
\text{Data rate} = \frac{f_{ADCK}}{\text{CHOP} \times \text{OSR}} = \frac{f_{MCLK}}{N \times \text{CHOP} \times \text{OSR}}
\]

\( f_{MCLK} \) is set in Step 5, the CHOP and N value are determined by the ADCR1 register setting, \( \text{OSR} \) is selected using the ADCR0 register.

Step 7: Enable the A/D converter by setting ADOFF = 0 and ADSLP = 0 in the ADCR0 register.

START
Step 8: Set the ADRST bit from low to high and then low again to reset the SINC filter.
Step 9: If the interrupts are to be used, set both the EMI and ADE bits high.
Step 10: If the interrupts are not used, users also can check when the A/D conversion process is complete by polling the EOC bit in the ADCR1 register. When this bit goes low, the conversion process has completed. Before reading the A/D data registers ADRL, ADRM and ADRH to obtain the conversion value, the ADCDL bit must be first set high. After the converted data has been read out, the ADCDL bit can then be cleared to zero.

Special Notes
For the 24-bit A/D Converter, there is a latency of four data conversion times between sampling and the converted data output. This means the converted data of the first sample will be output after the fourth conversion has completed, during which time the first three conversion results are unknown. The converted data of the second sample will be output after the fifth conversion has been completed, and so on.

All the input signal voltages should meet the following two conditions:
1. AN0 or AN1 should be in the range: 0.4V \( \sim \) (VOREG -1.1V)
2. (1) If AN0 > AN1, VOREG > VON = AN1 - (AN0 - AN1) / 2 \times (Gain - 1) \( \geq \) 0
   (2) If AN0 < AN1, VOREG > VOP = AN0 + (AN0 - AN1) / 2 \times (Gain - 1) \( \geq \) 0

When using an external reference voltage, the value of \( \Delta V_{REF} \times V_{REGN} \) must be noted to meet the following requirement.

<table>
<thead>
<tr>
<th>( V_{REF} )</th>
<th>( 0.96% )</th>
<th>1.25%</th>
<th>1.44%</th>
<th>V_{\text{REF}}</th>
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<tr>
<td>( V_{\text{REF}} )</td>
<td>( 0 )</td>
<td>( 0.08 )</td>
<td>( 0.125 )</td>
<td>( 0.144 )</td>
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Reference Circuit

Program Example

ha0416.zip

Conclusion

This application note has introduced the operating principles and usage method of the 24-bit A/D converter. With this description users should be able to quickly grasp how to use the HOLTEK 24-bit A/D converter.

Versions and Revision

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<th>Date</th>
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<tr>
<td>2016.02.17</td>
<td>陳振隆</td>
<td>First Version</td>
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Reference Files

Reference file: HT67F5650 DataSheet.
For more information, refer to the Holtek’s official website www.holtek.com.

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